TMR3 - Dual Timer Unit

Summary

This document provides detailed reference information with respect to the non-Wishbone dual timer unit peripheral component, TMR3.

The dual timer unit peripheral component (TMR3) is used to provide additional functionality to processor devices that do not inherently contain dedicated timing units. The peripheral can be configured as counters or timers and provides four distinct modes of operation.

Features

- Four 8-bit registers providing dual timer functionality
  - TLA, THA – constituting Timer A
  - TLB, THB – constituting Timer B
- Configurable functionality – either Timer or Counter
- Four modes of operation for each Timer/Counter
  - Mode 0 : 13-bit Timer/Counter
  - Mode 1 : 16-bit Timer/Counter
  - Mode 2 : 8-bit auto-reload Timer/Counter
  - Mode 3 : Timer/Counter B stopped. Timer/Counter A functions as two independent 8-bit Timers/Counters
- External timer clocking inputs with falling edge detection
- Ability to control Timer clocking via external enable input

Availability

From a schematic document, the TMR3 component can be found in the FPGA Peripherals integrated library (`FPGA Peripherals.IntLib`), located in the `\Library\Fpga` folder of the installation.

Functional Description

Symbol

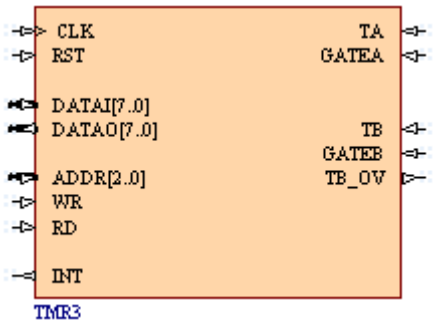

Figure 1. TMR3 symbol.

Pin Description

Table 1. TMR3 pin description

Name	Type	Polarity/Bus size	Description
Control Signals			
CLK	I	Rise	External system clock
RST	I	High	External system reset
Processor Interface Signals			
DATAI	I	8	Data received from host processor
DATAO	O	8	Data to be sent to host processor
ADDR	I	3	Address bus, used to select an internal register of the device for writing to/reading from.
WR	I	High	Write enable signal. When active, data can be written to an internal register of the device.
RD	I	High	Read enable signal. When active, data can be read from an internal register of the device.
INT	O	High	Interrupt signal. If either Timer A or Timer B have reached overflow state (i.e. either of the corresponding overflow bits in the Timer Control register are set), this signal is activated. This alerts the host to the fact that the timer/counter has reached its upper limit and has rolled over to start counting from zero.
Timer Input Signals			
TA	I	Fall	Timer A external clock input
GATEA	I	High	External Timer A enable input. If bit 3 of the Timer Mode register is set (1), Timer A is enabled solely by this external input.
TB	I	Fall	Timer B external clock input
GATEB	I	High	External Timer B enable input. If bit 7 of the Timer Mode register is set (1), Timer B is enabled solely by this external input.

Name	Type	Polarity/Bus size	Description
Timer Output Signals			
TB_OV	O	High	Timer B overflow output. This signal is taken high for a single period of the external system clock signal (CLK) when: TLB register (low byte of Timer B) reaches overflow state and current mode is mode 2. THB register (high byte of Timer B) reaches overflow state and current mode is mode 0,1 or 3.

Hardware Description

Block Diagram

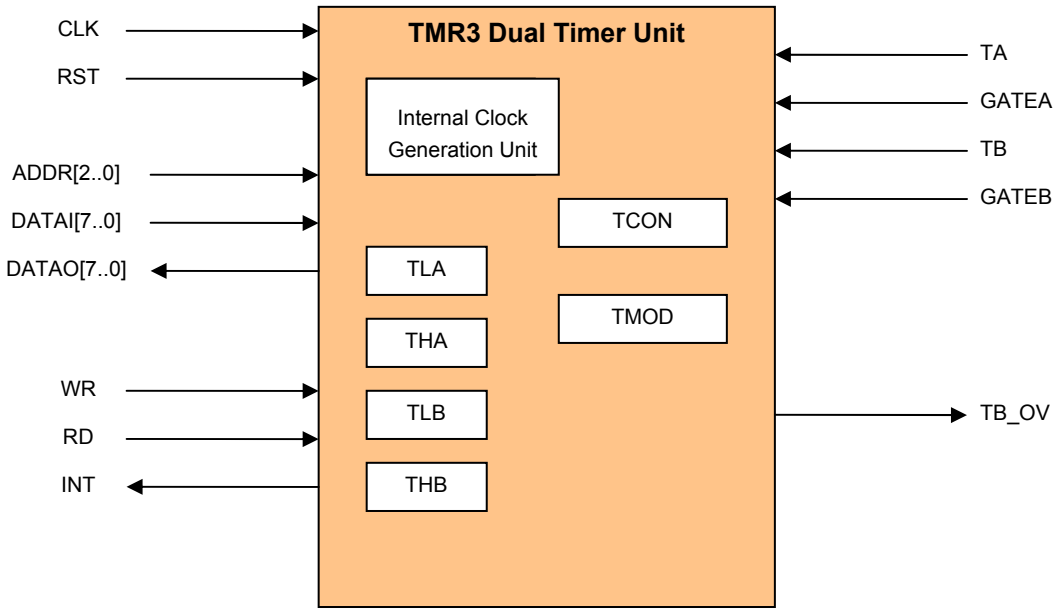

Figure 2. TMR3 block diagram

The TMR3 has two 16-bit registers: Timer A and Timer B. Both registers are further sub-divided into two 8-bit registers – TLA and TLB (low 8 bits); THA and THB (high 8 bits).

Both registers can be configured for counter or timer operations.

In timer mode, the register is incremented after every 12 cycles of the external system clock (CLK) signal. The required clock signal for each timer is obtained from the Internal Clock Generation Unit. This unit essentially provides a divide by 12 counter, whose input is the CLK signal and whose outputs are the internal clock signals TA_CLK and TB_CLK.

In counter mode, the register is incremented when a falling edge is observed at the corresponding external input pin (TA or TB). The maximum input count rate is 1/24 of the external clock frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least one period of the external clock signal.

Special Function Registers

Four operating modes can be selected for Timer A and Timer B. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

Timer Mode Register (TMOD)

Table 2. The TMOD register

MSB LSB

GATE	C/T	M1	M0	GATE	C/T	M1	M0
Timer B				**Timer A**			

Table 3. The TMOD register bits description

Bit	Symbol	Function
TMOD.3 TMOD.7	GATE	If set, enables external gate control (pin GATEA or GATEB for Timer/Counter A or B, respectively). When GATEA or GATEB is Low, and TRx bit is set (see TCON register), a timer/counter is incremented every falling edge on TA or TB input pin
TMOD.2 TMOD.6	C/T	Selects Timer or Counter operation. When set to 1, a Counter operation is performed, when cleared to 0, the corresponding register will function as a Timer.
TMOD.1 TMOD.5	M1	Selects mode for Timer/Counter A or Timer/Counter B, as shown in Table 4.
TMOD.0 TMOD.4	M0	Selects mode for Timer/Counter A or Timer/Counter B, as shown in Table 4.

Table 4. Timers/Counters Mode description

M1	M0	Mode	Function
0	0	Mode 0	13-bit Timer/Counter, with 5 lower bits in TLA or TLB register and 8 bits in THA or THB register (for Timer A and Timer B, respectively). The 3 high order bits of TLA and TLB are held at zero.
0	1	Mode 1	16-bit Timer/Counter.
1	0	Mode2	8 -bit auto-reload Timer/Counter. The reload value is kept in THA or THB, while TLA or TLB is incremented after every period of the external clock signal (CLK). When TLA/TLB overflows, a value from THA/THB is copied to TLA/TLB.
1	1	Mode3	If Timer B M1 and M0 bits are set to 1, Timer B stops. If Timer A M1 and M0 bits are set to 1, Timer A functions as follows: TLA operates as an 8-bit timer/counter THA operates as an 8-bit timer Both registers function independently of each other.

Note: When Timer A is configured in mode 3:

TLA is affected by the TRA and GATE control bits (TCON register), and sets TFA flag (TCON register) on overflow.

THA is affected by TRB bit, and sets TFB flag on overflow. (Both of these bits are in the TCON register).

Timer Control Register (TCON)

Table 5. The TCON register

MSB LSB

TFB	TRB	TFA	TRA	X	X	X	X

Table 6. The TCON register bit functions

Bit	Symbol	Function
TCON.7	TFB	Timer B overflow flag set by hardware when Timer B overflows. This flag should be cleared by the host processor.
TCON.6	TRB	Timer B Run control bit. If cleared, Timer B stops.
TCON.5	TFA	Timer A overflow flag set by hardware when Timer A overflows. This flag should be cleared by the host processor.
TCON.4	TRA	Timer A Run control bit. If cleared, Timer A stops.
TCON.3	X	Not used.
TCON.2	X	Not used.
TCON.1	X	Not used.
TCON.0	X	Not used.

Register Reset Values

Table 7 shows the values contained in each of the TMR3's internal registers after an external system reset has been received on the RST input.

Table 7. Register reset values

Register	Value after reset
TLA	00h
THA	00h
TLB	00h
THB	00h
TMOD	00h
TCON	00h

Timer Clocking and Interrupt Output Generation

Figure 3 presents a more detailed block diagram of the TMR3, showing the clocking of the two timers and the ultimate generation of the interrupt signal to the host processor – INT.

As can be seen in the diagram, both timers can be clocked by either an internal derivative of the external system clock, or by the falling edge of the relevant external input signal. The particular clocking signal used depends on whether the timer is configured in Timer or Counter mode respectively.

The clocking signal to Timer A is enabled when bit 4 of the TCON register (TRA) is '1' and either bit 3 of the TMOD register (GATE) is '0' or the external enable signal GATEA is '1'. If TMOD.3 is set (1), Timer A will be solely enabled by the GATEA signal.

Similarly, the clocking signal to Timer B is enabled when bit 6 of the TCON register (TRB) is '1' and either bit 7 of the TMOD register (GATE) is '0' or the external enable signal GATEB is '1'. To control Timer B using solely the GATEB signal, TMOD.7 must be set (1).

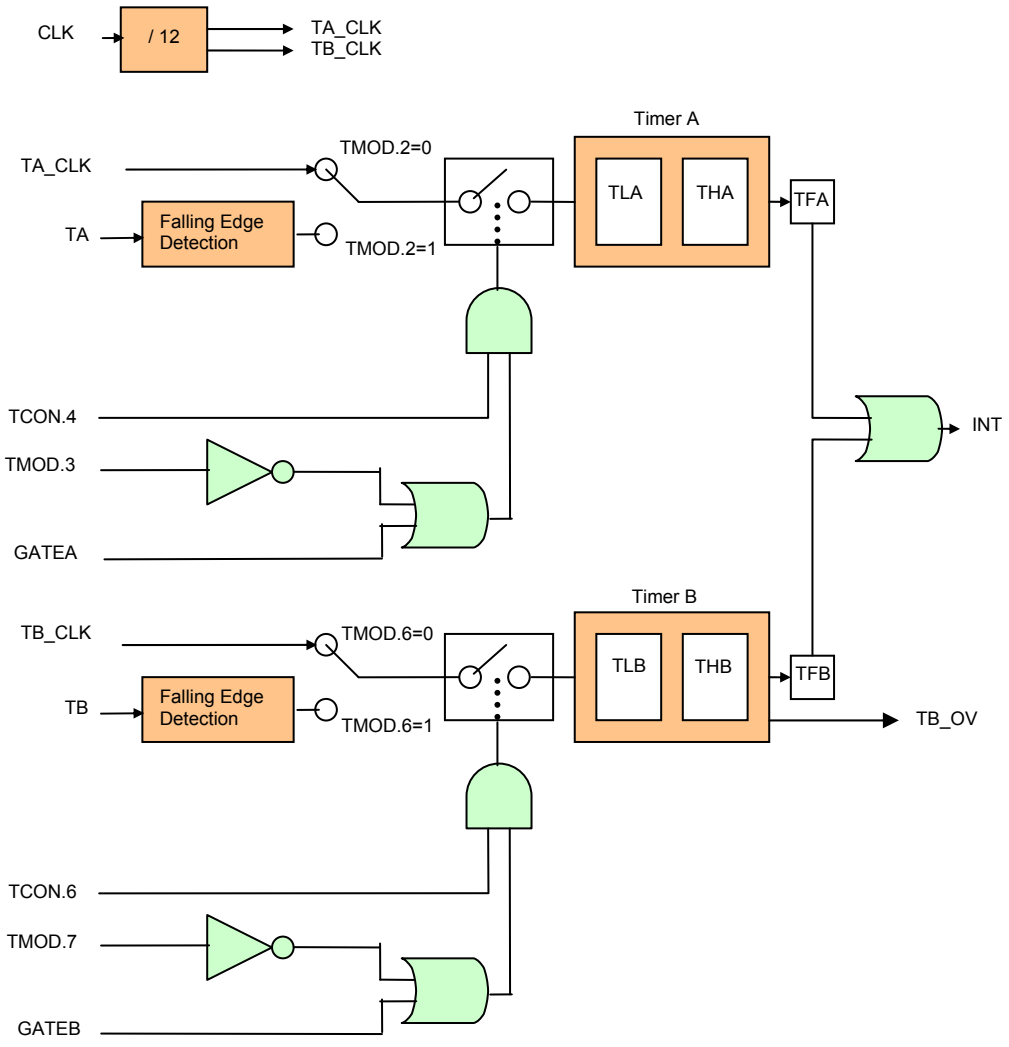

Figure 3. Timer clocking and interrupt output generation

Reading/Writing the Internal Registers

The host processor can read/write any of the TMR3's internal registers. Selection of a particular register is achieved by supplying the unique, 3-bit binary ID address code of the register. This code is sent to the TMR3 and appears at the ADDR input. Table 8 shows the unique address IDs associated with each of the registers.

Table 8. Internal register unique address IDs

Register	Unique Register Address ID
TLA	010
THA	100
TLB	011
THB	101
TMOD	001
TCON	000

Writing to the Timer Control Register (TCON)

The TCON register can be written to in the following circumstances. In each case, the write operation occurs on the rising edge of the CLK input.

System Reset

After reception of an external system reset (RST goes High), the TCON register is loaded with the reset value 00h.

Host Processor Write

Data can be written from the host processor to the TCON register. This data transfer cycle can be summarized as follows:

- The host writes the unique 3-bit address ID for the TCON register (000) to the ADDR input of the TMR3
- The host sends a valid byte of data to the TMR3's DATAI input
- The host then sets the TMR3's WR signal High, to specify a Write cycle
- The TMR3 latches the byte of data into the TCON register.

Timer A Overflow

If Timer A is in either mode 0 or mode 1 and register THA has reached the overflow state, then bit 5 (TFA) of the TCON register is set (1).

Similarly, this bit of the TCON register will also be set (1) if Timer A is in either mode 0 or mode 1 and register TLA has reached the overflow state.

Timer B Overflow

Bit 7 (TFB) of the TCON register will be set under the following conditions:

- If Timer B is in either mode 0 or mode 1 and register THB has reached the overflow state.
- If Timer B is in mode 2 and register TLB has reached the overflow state.
- If Timer A is in mode 3 and register THA has reached the overflow state.

Writing to the Timer Mode Register (TMOD)

The TMOD register can be written to in the following circumstances. In each case, the write operation occurs on the rising edge of the CLK input.

System Reset

After reception of an external system reset (RST goes High), the TMOD register is loaded with the reset value 00h.

Host Processor Write

This data transfer cycle can be summarized as follows:

- The host writes the unique 3-bit address ID for the TMOD register (001) to the ADDR input of the TMR3
- The host sends a valid byte of data to the TMR3's DATAI input
- The host then sets the TMR3's WR signal High, to specify a Write cycle
- The TMR3 latches the byte of data into the TMOD register.

Writing to Timer A

Timer A (registers TLA and THA) can be written to in the following circumstances. In each case, the write operation occurs on the rising edge of the CLK input.

System Reset

After reception of an external system reset (RST goes High), the TLA and THA registers are loaded with the reset value 00h.

Writing to the TLA Register

Host Processor Write

This data transfer cycle can be summarized as follows:

- The host writes the unique 3-bit address ID for the TLA register (010) to the ADDR input of the TMR3
- The host sends a valid byte of data to the TMR3's DATAI input
- The host then sets the TMR3's WR signal High, to specify a Write cycle
- The TMR3 latches the data into the TLA register

The actual value loaded into the TLA register depends on the current mode setting for Timer A. If the current mode is mode 0, the top three bits of TLA are loaded with zeros, whilst bits 4-0 are loaded with the corresponding bit values from the byte of data arriving from the host at the DATAI input. If the current mode is mode 1,2 or 3, TLA is loaded with the complete byte of data sent from the host.

Auto-Reload (Mode 2)

When Timer A is currently in mode 2 and the TLA register reaches the overflow state, the reload value stored in the THA register will be automatically loaded into the TLA register.

TLA Register Active Clock Signal (Modes 0,1,3)

The content of the TLA register will be incremented by 1 when the register's clock input (TLA_CLK) goes High. The nature of the increment depends on the current mode setting for Timer A:

- In mode 0, the value represented by the low 5 bits of TLA is incremented by 1 – bits 7-5 are held constantly at 0.
- In modes 1 and 3, the full value in the TLA register is incremented by 1.

Writing to the THA Register

Host Processor Write

This data transfer cycle can be summarized as follows:

- The host writes the unique 3-bit address ID for the THA register (100) to the ADDR input of the TMR3
- The host sends a valid byte of data to the TMR3's DATAI input
- The host then sets the TMR3's WR signal High, to specify a Write cycle
- The TMR3 latches the data into the THA register.

THA is loaded with the complete byte of data from the host, irrespective of the current mode setting for Timer A.

THA Register Active Clock Signal

The content of the THA register will be incremented by 1 when the register's clock input (THA_CLK) goes High.

Writing to Timer B

Timer B (registers TLB and THB) can be written to in the following circumstances. In each case, the write operation occurs on the rising edge of the CLK input.

System Reset

After reception of an external system reset (RST goes High), the TLB and THB registers are loaded with the reset value 00h.

Writing to the TLB Register

Host Processor Write

This data transfer cycle can be summarized as follows:

- The host writes the unique 3-bit address ID for the TLB register (011) to the ADDR input of the TMR3
- The host sends a valid byte of data to the TMR3's DATAI input
- The host then sets the TMR3's WR signal High, to specify a Write cycle
- The TMR3 latches the data into the TLB register.

The actual value loaded into the TLB register depends on the current mode setting for Timer B. If the current mode is mode 0, the top three bits of TLB are loaded with zeros, whilst bits 4-0 are loaded with the corresponding bit values from the byte of data arriving from the host at the DATAI input. If the current mode is mode 1,2 or 3, TLB is loaded with the complete byte of data sent from the host.

Auto-Reload (Mode 2

When Timer B is currently in mode 2 and the TLB register reaches the overflow state, the reload value stored in the THB register will be automatically loaded into the TLB register.

TLB Register Active Clock Signal (Modes 0,1,3)

The content of the TLB register will be incremented by 1 when the register's clock input (TLB_CLK) goes High. The nature of the increment depends on the current mode setting for Timer B:

- In mode 0, the value represented by the low 5 bits of TLB is incremented by 1 – bits 7-5 are held constantly at 0.
- In modes 1 and 3, the full value in the TLB register is incremented by 1.

Writing to the THB Register

Host Processor Write

This data transfer cycle can be summarized as follows:

- The host writes the unique 3-bit address ID for the THB register (101) to the ADDR input of the TMR3
- The host sends a valid byte of data to the TMR3's DATAI input
- The host then sets the TMR3's WR signal High, to specify a Write cycle
- The TMR3 latches the data into the THB register.

THB is loaded with the complete byte of data from the host, irrespective of the current mode setting for Timer B.

THB Register Active Clock Signal

The content of the THB register will be incremented by 1 when the register's clock input (THB_CLK) goes High AND the current mode setting for Timer B is either 0,1 or 3.

Reading from the Internal Registers

Data can be read from one of the TMR3's internal registers. This data transfer cycle can be summarized as follows:

- The host writes the unique 3-bit address ID for the internal register to be read (see Table 16) to the ADDR input of the TMR3
- The host then sets the TMR3's RD signal High, to specify a Read cycle
- The TMR3 presents the byte of data from the chosen register at the DATAO output.

Revision History

Date	Version No.	Revision
12-Feb-2009	1.0	Initial document release
30-Aug-2011	-	Updated template.