



FPGA Wired Function Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Wired Function cores.

Core Reference
CR0143 (v1.11) December 19, 2008

Wired Function

The available Wired Function cores are listed as follows:

<i>PULLDOWN</i>	<i>PULLDOWN4B</i>	<i>PULLDOWN4S</i>	<i>PULLDOWN8B</i>
<i>PULLDOWN8S</i>	<i>PULLDOWN12B</i>	<i>PULLDOWN12S</i>	<i>PULLDOWN16B</i>
<i>PULLDOWN16S</i>	<i>PULLDOWN32B</i>	<i>PULLUP</i>	<i>PULLUP4B</i>
<i>PULLUP4S</i>	<i>PULLUP8B</i>	<i>PULLUP8S</i>	<i>PULLUP12B</i>
<i>PULLUP12S</i>	<i>PULLUP16B</i>	<i>PULLUP16S</i>	<i>PULLUP32B</i>

FPGA Wired Function Resource Usage

PULLDOWN

Level Low

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		1	1										
Cyclone2		1											
Cyclone3													
Stratix		1											
Stratix2		1											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2	1	1											
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1											
Spartan2E		1											
Spartan3		1											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		1	1										
Spartan3L													
Virtex		1											
Virtex2		1											
Virtex2p		1											
VirtexE		1											
Virtex4		1											
Virtex5													
CoolRunner2	1	1											
CoolRunnerXpla3	1	1											
Xc9500	1	1											
Xc9500XL	1	1											
Xc9500XV	1	1											
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion													
EC		1	1										
ECP		1	1										
ECP2		2	1										
ECP2M		2	1										
SC													
MACHXO													
XP													
XP2		2	1										

PULLDOWN4B

4-Bit Level Low Bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		4	4										
Cyclone2		4											
Cyclone3													
Stratix		4											
Stratix2		4											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4											
Spartan2E		4											
Spartan3		4											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		4	4										
Spartan3L													
Virtex		4											
Virtex2		4											
Virtex2p		4											
VirtexE		4											
Virtex4		4											
Virtex5													
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus	4	4											
ProAsic3	4	4											
ProAsic3E	4	4											
Fusion													
EC		4	4										
ECP		4	4										
ECP2		2	1										
ECP2M		2	1										
SC													
MACHXO													
XP													
XP2		2	1										

FPGA Wired Function Resource Usage

PULLDOWN4S

4-Bit Level Low

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		4	4										
Cyclone2		4											
Cyclone3													
Stratix		4											
Stratix2		4											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4											
Spartan2E		4											
Spartan3		4											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		4	4										
Spartan3L													
Virtex		4											
Virtex2		4											
Virtex2p		4											
VirtexE		4											
Virtex4		4											
Virtex5													
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus	4	4											
ProAsic3	4	4											
ProAsic3E	4	4											
Fusion													
EC		4	4										
ECP		4	4										
ECP2		2	1										
ECP2M		2	1										
SC													
MACHXO													
XP													
XP2		2	1										

PULLDOWN8B

8-Bit Level Low Bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		8	8										
Cyclone2		8											
Cyclone3													
Stratix		8											
Stratix2		8											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8											
Spartan2E		8											
Spartan3		8											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		8											
Spartan3L													
Virtex		8											
Virtex2		8											
Virtex2p		8											
VirtexE		8											
Virtex4		8											
Virtex5													
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus	8	8											
ProAsic3	8	8											
ProAsic3E	8	8											
Fusion													
EC		8	8										
ECP		8	8										
ECP2		2	1										
ECP2M		2	1										
SC													
MACHXO													
XP													
XP2		2	1										

FPGA Wired Function Resource Usage

PULLDOWN8S

8-Bit Level Low

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		8	8										
Cyclone2		8											
Cyclone3													
Stratix		8											
Stratix2		8											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8											
Spartan2E		8											
Spartan3		8											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		8											
Spartan3L													
Virtex		8											
Virtex2		8											
Virtex2p		8											
VirtexE		8											
Virtex4		8											
Virtex5													
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus	8	8											
ProAsic3	8	8											
ProAsic3E	8	8											
Fusion													
EC		8	8										
ECP		8	8										
ECP2		2	1										
ECP2M		2	1										
SC													
MACHXO													
XP													
XP2		2	1										

PULLDOWN12B

12-Bit Level Low Bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		12	12										
Cyclone2		12											
Cyclone3													
Stratix		12											
Stratix2		12											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12											
Spartan2E		12											
Spartan3		12											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		12											
Spartan3L													
Virtex		12											
Virtex2		12											
Virtex2p		12											
VirtexE		12											
Virtex4		12											
Virtex5													
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion													
EC		12	12										
ECP		12	12										
ECP2		2	1										
ECP2M		2	1										
SC													
MACHXO													
XP													
XP2		2	1										

FPGA Wired Function Resource Usage

PULLDOWN12S

12-Bit Level Low

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		12	12										
Cyclone2		12											
Cyclone3													
Stratix		12											
Stratix2		12											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12											
Spartan2E		12											
Spartan3		12											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		12											
Spartan3L													
Virtex		12											
Virtex2		12											
Virtex2p		12											
VirtexE		12											
Virtex4		12											
Virtex5													
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion													
EC		12	12										
ECP		12	12										
ECP2		2	1										
ECP2M		2	1										
SC													
MACHXO													
XP													
XP2		2	1										

PULLDOWN16B

16-Bit Level Low Bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		16	16										
Cyclone2		16											
Cyclone3													
Stratix		16											
Stratix2		16											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2	16	16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16											
Spartan2E		16											
Spartan3		16											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E	16	16											
Spartan3L													
Virtex		16											
Virtex2		16											
Virtex2p		16											
VirtexE		16											
Virtex4		16											
Virtex5													
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion													
EC		16											
ECP		16											
ECP2		2	1										
ECP2M		2	1										
SC													
MACHXO													
XP													
XP2		2	1										

FPGA Wired Function Resource Usage

PULLDOWN16S

16-Bit Level Low

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		16	16										
Cyclone2		16											
Cyclone3													
Stratix		16											
Stratix2		16											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2	16	16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16											
Spartan2E		16											
Spartan3		16											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E	16	16											
Spartan3L													
Virtex		16											
Virtex2		16											
Virtex2p		16											
VirtexE		16											
Virtex4		16											
Virtex5													
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion													
EC		16											
ECP		16											
ECP2		2	1										
ECP2M		2	1										
SC													
MACHXO													
XP													
XP2		2	1										

PULLDOWN32B

32-Bit Level Low Bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		32	32										
Cyclone2		32											
Cyclone3													
Stratix		32											
Stratix2		32											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2	32	32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32											
Spartan2E		32											
Spartan3		32											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		32	32										
Spartan3L													
Virtex		32											
Virtex2		32											
Virtex2p		32											
VirtexE		32											
Virtex4		32											
Virtex5													
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		32											
Fusion													
EC		32	32										
ECP		32	32										
ECP2		2	1										
ECP2M		2	1										
SC													
MACHXO													
XP													
XP2		2	1										

FPGA Wired Function Resource Usage

PULLUP

Level High

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		1	1										
Cyclone2		1											
Cyclone3													
Stratix		1											
Stratix2		1											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2	1	1											
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1											
Spartan2E		1											
Spartan3		1											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		1	1										
Spartan3L													
Virtex		1											
Virtex2		1											
Virtex2p		1											
VirtexE		1											
Virtex4		1											
Virtex5													
CoolRunner2	1	1											
CoolRunnerXpla3	1	1											
Xc9500	1	1											
Xc9500XL	1	1											
Xc9500XV	1	1											
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion													
EC		1	1										
ECP		1	1										
ECP2													
ECP2M													
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2													

PULLUP4B

4-Bit Level High Bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		4	4										
Cyclone2		4											
Cyclone3													
Stratix		4											
Stratix2		4											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4											
Spartan2E		4											
Spartan3		4											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		4	4										
Spartan3L													
Virtex		4											
Virtex2		4											
Virtex2p		4											
VirtexE		4											
Virtex4		4											
Virtex5													
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus	4	4											
ProAsic3	4	4											
ProAsic3E	4	4											
Fusion													
EC		4	4										
ECP		4	4										
ECP2													
ECP2M													
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2													

FPGA Wired Function Resource Usage

PULLUP4S

4-Bit Level High

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		4	4										
Cyclone2		4											
Cyclone3													
Stratix		4											
Stratix2		4											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4											
Spartan2E		4											
Spartan3		4											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		4	4										
Spartan3L													
Virtex		4											
Virtex2		4											
Virtex2p		4											
VirtexE		4											
Virtex4		4											
Virtex5													
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus	4	4											
ProAsic3	4	4											
ProAsic3E	4	4											
Fusion													
EC		4	4										
ECP		4	4										
ECP2													
ECP2M													
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2													

PULLUP8B

8-Bit Level High Bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		8	8										
Cyclone2		8											
Cyclone3													
Stratix		8											
Stratix2		8											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8											
Spartan2E		8											
Spartan3		8											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		8											
Spartan3L													
Virtex		8											
Virtex2		8											
Virtex2p		8											
VirtexE		8											
Virtex4		8											
Virtex5													
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus	8	8											
ProAsic3	8	8											
ProAsic3E	8	8											
Fusion													
EC		8	8										
ECP		8	8										
ECP2													
ECP2M													
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2													

FPGA Wired Function Resource Usage

PULLUP8S

8-Bit Level High

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		8	8										
Cyclone2		8											
Cyclone3													
Stratix		8											
Stratix2		8											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8											
Spartan2E		8											
Spartan3		8											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		8											
Spartan3L													
Virtex		8											
Virtex2		8											
Virtex2p		8											
VirtexE		8											
Virtex4		8											
Virtex5													
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus	8	8											
ProAsic3	8	8											
ProAsic3E	8	8											
Fusion													
EC		8	8										
ECP		8	8										
ECP2													
ECP2M													
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2													

PULLUP12B

12-Bit Level High Bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		12	12										
Cyclone2		12											
Cyclone3													
Stratix		12											
Stratix2		12											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12											
Spartan2E		12											
Spartan3		12											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		12											
Spartan3L													
Virtex		12											
Virtex2		12											
Virtex2p		12											
VirtexE		12											
Virtex4		12											
Virtex5													
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion													
EC		12	12										
ECP		12	12										
ECP2													
ECP2M													
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2													

FPGA Wired Function Resource Usage

PULLUP12S

12-Bit Level High

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		12	12										
Cyclone2		12											
Cyclone3													
Stratix		12											
Stratix2		12											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12											
Spartan2E		12											
Spartan3		12											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		12											
Spartan3L													
Virtex		12											
Virtex2		12											
Virtex2p		12											
VirtexE		12											
Virtex4		12											
Virtex5													
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion													
EC		12	12										
ECP		12	12										
ECP2													
ECP2M													
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2													

PULLUP16B

16-Bit Level High Bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		16	16										
Cyclone2		16											
Cyclone3													
Stratix		16											
Stratix2		16											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2	16	16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16											
Spartan2E		16											
Spartan3		16											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		16	16										
Spartan3L													
Virtex		16											
Virtex2		16											
Virtex2p		16											
VirtexE		16											
Virtex4		16											
Virtex5													
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion													
EC		16											
ECP		16											
ECP2													
ECP2M													
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2													

FPGA Wired Function Resource Usage

PULLUP16S

16-Bit Level High

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		16	16										
Cyclone2		16											
Cyclone3													
Stratix		16											
Stratix2		16											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2	16	16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16											
Spartan2E		16											
Spartan3		16											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E	16	16											
Spartan3L													
Virtex		16											
Virtex2		16											
Virtex2p		16											
VirtexE		16											
Virtex4		16											
Virtex5													
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion													
EC		16											
ECP		16											
ECP2													
ECP2M													
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2													

PULLUP32B

32-Bit Level High Bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx													
Cyclone		32	32										
Cyclone2		32											
Cyclone3													
Stratix		32											
Stratix2		32											
Stratix3													
StratixGX		1											
Stratix2GX													
Max2	32	32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32											
Spartan2E		32											
Spartan3		32											
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		32	32										
Spartan3L													
Virtex		32											
Virtex2		32											
Virtex2p		32											
VirtexE		32											
Virtex4		32											
Virtex5													
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		32											
Fusion													
EC		32	32										
ECP		32	32										
ECP2													
ECP2M													
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2													

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1

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