



## FPGA Shifter Resource Usage

### Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Shifter cores.

Core Reference  
CR0142 (v1.11) December 19, 2008

### Shifter

The available Shifter cores are listed as follows:

*BRLSHFT4B*

*BRLSHFT4S*

*BRLSHFT8B*

*BRLSHFT8S*

*BRLSHFT16B*

*BRLSHFT32B*

*BRLSHFTM4B*

*BRLSHFTM4S*

*BRLSHFTM8B*

*BRLSHFTM8S*

*BRLSHFTM16B*

*BRLSHFTM32B*

FPGA Shifter Resource Usage

**BRLSHFT4B**

**4-Bit Barrel Shifter, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6										
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		4	4										
Stratix3			6										
StratixGX		8	8										
Stratix2GX			6										
Max2		8	8										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		10	8										
Spartan2E		10	8										
Spartan3		10	8										
Spartan3A		10	8										
Spartan3ADSP		10	8										
Spartan3AN		10	8										
Spartan3E		10	8										
Spartan3L		10	8										
Virtex		10	8										
Virtex2		10	8										
Virtex2p		10	8										
VirtexE		10	8										
Virtex4		10	8										
Virtex5		8											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		12											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
SC		8	8										
MACHXO		8	8										
XP		8	8										
XP2		8	8										

## BRLSHFT4S

### 4-Bit Barrel Shifter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6										
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		4	4										
Stratix3			6										
StratixGX		8	8										
Stratix2GX			6										
Max2		8	8										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		10	8										
Spartan2E		10	8										
Spartan3		10	8										
Spartan3A		10	8										
Spartan3ADSP		10	8										
Spartan3AN		10	8										
Spartan3E		10	8										
Spartan3L		10	8										
Virtex		10	8										
Virtex2		10	8										
Virtex2p		10	8										
VirtexE		10	8										
Virtex4		10	8										
Virtex5		8											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		12											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
SC		8	8										
MACHXO		8	8										
XP		8	8										
XP2		8	8										

**FPGA Shifter Resource Usage**

**BRLSHFT8B**

**8-Bit Barrel Shifter, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			18										
Cyclone		24	24										
Cyclone2		24	24										
Cyclone3		24	24										
Stratix		24	24										
Stratix2		16	16										
Stratix3			18										
StratixGX		24	24										
Stratix2GX			18										
Max2		24	24										
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		24	24										
Spartan2E		24	24										
Spartan3		24	24										
Spartan3A		24	24										
Spartan3ADSP		24	24										
Spartan3AN		24	24										
Spartan3E		24	24										
Spartan3L		24	24										
Virtex		24	24										
Virtex2		24	24										
Virtex2p		24	24										
VirtexE		24	24										
Virtex4		24	24										
Virtex5		14											
CoolRunner2	8												
CoolRunnerXpla3	8												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		92											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		24	24										
ECP		24	24										
ECP2		24	24										
ECP2M		24	24										
SC		32	24										
MACHXO		24	24										
XP		24	24										
XP2		24	24										

## BRLSHFT8S

### 8-Bit Barrel Shifter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			18										
Cyclone		24	24										
Cyclone2		24	24										
Cyclone3		24	24										
Stratix		24	24										
Stratix2		16	16										
Stratix3			18										
StratixGX		24	24										
Stratix2GX			18										
Max2		24	24										
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		24	24										
Spartan2E		24	24										
Spartan3		24	24										
Spartan3A		24	24										
Spartan3ADSP		24	24										
Spartan3AN		24	24										
Spartan3E		24	24										
Spartan3L		24	24										
Virtex		24	24										
Virtex2		24	24										
Virtex2p		24	24										
VirtexE		24	24										
Virtex4		24	24										
Virtex5		12											
CoolRunner2	8												
CoolRunnerXpla3	8												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		92											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		24	24										
ECP		24	24										
ECP2		24	24										
ECP2M		24	24										
SC		32	24										
MACHXO		24	24										
XP		24	24										
XP2		24	24										

FPGA Shifter Resource Usage

**BRLSHFT16B**

**16-Bit Barrel Shifter, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			46										
Cyclone	64	64											
Cyclone2	64	64											
Cyclone3	64	64											
Stratix	64	64											
Stratix2	32	32											
Stratix3			46										
StratixGX	64	64											
Stratix2GX			46										
Max2	64	64											
Max3000a	64	64											
Max7000b	64	64											
Max7000ae	64	64											
Max7000s	64	64											
Spartan2	66	64											
Spartan2E	66	64											
Spartan3	68	65											
Spartan3A	68	65											
Spartan3ADSP	68	65											
Spartan3AN	68	65											
Spartan3E	68	65											
Spartan3L	68	67											
Virtex	66	64											
Virtex2	68	65											
Virtex2p	68	65											
VirtexE	66	64											
Virtex4	68	65											
Virtex5	26												
CoolRunner2	16												
CoolRunnerXpla3	16												
Xc9500	16												
Xc9500XL	16												
Xc9500XV	16												
ProAsicPlus		360											
ProAsic3	64												
ProAsic3E	68												
Fusion	64												
EC	64	64											
ECP	64	64											
ECP2	66	64											
ECP2M	66	64											
SC	64	64											
MACHXO	66	64											
XP	64	64											
XP2	66	64											

**BRLSHFT32B**

**32-Bit Barrel Shifter, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			119										
Cyclone		160	160										
Cyclone2		160	160										
Cyclone3		160	160										
Stratix		160	160										
Stratix2		96	96										
Stratix3			118										
StratixGX		160	160										
Stratix2GX			120										
Max2		160	160										
Max3000a	224	224											
Max7000b	224	224											
Max7000ae	224	224											
Max7000s	224	224											
Spartan2		166	164										
Spartan2E		166	164										
Spartan3		170	168										
Spartan3A		170	168										
Spartan3ADSP		170	168										
Spartan3AN		170	168										
Spartan3E		170	168										
Spartan3L		166	165										
Virtex		166	164										
Virtex2		170	168										
Virtex2p		170	168										
VirtexE		166	164										
Virtex4		170	168										
Virtex5		122											
CoolRunner2	44												
CoolRunnerXpla3	480												
Xc9500	47												
Xc9500XL	47												
Xc9500XV	47												
ProAsicPlus		160											
ProAsic3		170											
ProAsic3E		170											
Fusion		160											
EC		512	512										
ECP		512	512										
ECP2		192	160										
ECP2M		192	160										
SC		192	160										
MACHXO		192	160										
XP		192	160										
XP2		192	160										

FPGA Shifter Resource Usage

**BRLSHFTM4B**

**4-Bit Fill Mode Bi-Directional Barrel Shifter, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10										
Cyclone		17	17										
Cyclone2		17	17										
Cyclone3		18	18										
Stratix		17	17										
Stratix2		13	13										
Stratix3			10										
StratixGX		17	17										
Stratix2GX			9										
Max2		17	17										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		18	17										
Spartan2E		18	17										
Spartan3		18	17										
Spartan3A		18	17										
Spartan3ADSP		18	17										
Spartan3AN		18	17										
Spartan3E		18	17										
Spartan3L		18	17										
Virtex		18	17										
Virtex2		18	17										
Virtex2p		18	17										
VirtexE		18	17										
Virtex4		18	17										
Virtex5			8										
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		30											
ProAsic3		35											
ProAsic3E		25											
Fusion		25											
EC		18	15										
ECP		18	15										
ECP2		18	17										
ECP2M		18	17										
SC		18	16										
MACHXO		18	17										
XP		18	17										
XP2		18	17										



## BRLSHFTM4S

### 4-Bit Fill Mode Bi-Directional Barrel Shifter, Single pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10										
Cyclone		17	17										
Cyclone2		17	17										
Cyclone3		18	18										
Stratix		17	17										
Stratix2		13	13										
Stratix3			10										
StratixGX		17	17										
Stratix2GX			9										
Max2		17	17										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		18	17										
Spartan2E		18	17										
Spartan3		18	17										
Spartan3A		18	17										
Spartan3ADSP		18	17										
Spartan3AN		18	17										
Spartan3E		18	17										
Spartan3L		18	17										
Virtex		18	17										
Virtex2		18	17										
Virtex2p		18	17										
VirtexE		18	17										
Virtex4		18	17										
Virtex5			8										
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		30											
ProAsic3		35											
ProAsic3E		25											
Fusion		25											
EC		18	15										
ECP		18	15										
ECP2		18	17										
ECP2M		18	17										
SC		18	16										
MACHXO		18	17										
XP		18	17										
XP2		18	17										

FPGA Shifter Resource Usage

**BRLSHFTM8B**

**8-Bit Fill Mode Bi-Directional Barrel Shifter, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			39										
Cyclone		50	50										
Cyclone2		50	50										
Cyclone3		52	52										
Stratix		50	50										
Stratix2		35	35										
Stratix3			39										
StratixGX		50	50										
Stratix2GX			31										
Max2		50	50										
Max3000a	18	18											
Max7000b	18	18											
Max7000ae	18	18											
Max7000s	18	18											
Spartan2		46	45										
Spartan2E		46	45										
Spartan3		48	46										
Spartan3A		48	46										
Spartan3ADSP		48	46										
Spartan3AN		48	46										
Spartan3E		48	46										
Spartan3L		48	47										
Virtex		46	45										
Virtex2		48	46										
Virtex2p		48	46										
VirtexE		46	45										
Virtex4		48	46										
Virtex5		16											
CoolRunner2	8												
CoolRunnerXpla3	8												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		71											
ProAsic3		68											
ProAsic3E		69											
Fusion		65											
EC		60	53										
ECP		60	53										
ECP2		54	48										
ECP2M		54	48										
SC		56	49										
MACHXO		52	48										
XP		54	49										
XP2		54	48										

## BRLSHFTM8S

### 8-Bit Fill Mode Bi-Directional Barrel Shifter, Single pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			35										
Cyclone		50	50										
Cyclone2		50	50										
Cyclone3		52	52										
Stratix		50	50										
Stratix2		35	35										
Stratix3			35										
StratixGX		50	50										
Stratix2GX			34										
Max2		50	50										
Max3000a	18	18											
Max7000b	18	18											
Max7000ae	18	18											
Max7000s	18	18											
Spartan2		46	46										
Spartan2E		46	46										
Spartan3		48	47										
Spartan3A		48	47										
Spartan3ADSP		46	45										
Spartan3AN		48	47										
Spartan3E		48	47										
Spartan3L		46	45										
Virtex		46	46										
Virtex2		48	47										
Virtex2p		48	47										
VirtexE		46	46										
Virtex4		48	47										
Virtex5		18											
CoolRunner2	8												
CoolRunnerXpla3	8												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		71											
ProAsic3		68											
ProAsic3E		69											
Fusion		65											
EC		58	53										
ECP		58	53										
ECP2		52	47										
ECP2M		52	47										
SC		54	48										
MACHXO		50	48										
XP		54	48										
XP2		52	47										

**FPGA Shifter Resource Usage**

**BRLSHFTM16B**

**16-Bit Fill Mode Bi-Directional Barrel Shifter, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			93										
Cyclone		138	138										
Cyclone2		130	130										
Cyclone3		135	135										
Stratix		138	138										
Stratix2		81	81										
Stratix3			93										
StratixGX		138	138										
Stratix2GX			95										
Max2		154	154										
Max3000a	64	64											
Max7000b	64	64											
Max7000ae	64	64											
Max7000s	64	64											
Spartan2		130	128										
Spartan2E		130	128										
Spartan3		128	127										
Spartan3A		130	129										
Spartan3ADSP		128	128										
Spartan3AN		130	129										
Spartan3E		128	127										
Spartan3L		128	128										
Virtex		130	128										
Virtex2		128	127										
Virtex2p		128	127										
VirtexE		130	128										
Virtex4		128	127										
Virtex5		70											
CoolRunner2	16												
CoolRunnerXpla3	16												
Xc9500	16												
Xc9500XL	16												
Xc9500XV	16												
ProAsicPlus		175											
ProAsic3		170											
ProAsic3E		174											
Fusion		162											
EC		150	143										
ECP		150	143										
ECP2		142	130										
ECP2M		142	130										
SC		146	129										
MACHXO		142	128										
XP		140	128										
XP2		142	129										

**BRLSHFTM32B**

**32-Bit Fill Mode Bi-Directional Barrel Shifter, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			234										
Cyclone		340	340										
Cyclone2		329	329										
Cyclone3		332	332										
Stratix		340	340										
Stratix2		202	202										
Stratix3			234										
StratixGX		340	340										
Stratix2GX			249										
Max2		367	367										
Max3000a	272	272											
Max7000b	272	272											
Max7000ae	272	272											
Max7000s	256	256											
Spartan2		326	319										
Spartan2E		326	319										
Spartan3		328	326										
Spartan3A		330	325										
Spartan3ADSP		330	321										
Spartan3AN		330	325										
Spartan3E		328	326										
Spartan3L		320	318										
Virtex		326	319										
Virtex2		328	326										
Virtex2p		328	326										
VirtexE		326	319										
Virtex4		328	326										
Virtex5		162											
CoolRunner2	64												
CoolRunnerXpla3	1030												
Xc9500	87												
Xc9500XL	77												
Xc9500XV	77												
ProAsicPlus		412											
ProAsic3		390											
ProAsic3E		392											
Fusion		387											
EC		390	356										
ECP		390	356										
ECP2		368	316										
ECP2M		368	316										
SC		378	319										
MACHXO		370	321										
XP		358	318										
XP2		358	321										

## Tools Utilized

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The following vendor device tools were used to determine the resource usage statistics:

### **Actel**

Actel Designer Software Version 6.2

### **Altera**

Quartus II 5.0

### **Lattice**

ispLEVER 5.0

### **Xilinx**

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

## Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1

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