



FPGA Shift Register Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Shift Register cores.

Core Reference
CR0141 (v1.11) December 19, 2008

Shift Register

The available Shift Register cores are listed as follows:

<i>SR4CEB</i>	<i>SR4CES</i>	<i>SR4CLEB</i>	<i>SR4CLEDB</i>
<i>SR4CLEDS</i>	<i>SR4CLES</i>	<i>SR4REB</i>	<i>SR4RES</i>
<i>SR4RLEB</i>	<i>SR4RLEDB</i>	<i>SR4RLEDS</i>	<i>SR4RLES</i>
<i>SR8CEB</i>	<i>SR8CES</i>	<i>SR8CLEB</i>	<i>SR8CLEDB</i>
<i>SR8CLEDS</i>	<i>SR8CLES</i>	<i>SR8REB</i>	<i>SR8RES</i>
<i>SR8RLEB</i>	<i>SR8RLEDB</i>	<i>SR8RLEDS</i>	<i>SR8RLES</i>
<i>SR16CEB</i>	<i>SR16CES</i>	<i>SR16CLEB</i>	<i>SR16CLEDB</i>
<i>SR16CLEDS</i>	<i>SR16CLES</i>	<i>SR16REB</i>	<i>SR16RES</i>
<i>SR16RLEB</i>	<i>SR16RLEDB</i>	<i>SR16RLEDS</i>	<i>SR16RLES</i>
<i>SR32CEB</i>	<i>SR32CLEB</i>	<i>SR32CLEDB</i>	<i>SR32REB</i>
<i>SR32RLEB</i>	<i>SR32RLEDB</i>		

FPGA Shift Register Resource Usage

SR4CEB

4-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4									
Cyclone		4	4								2	
Cyclone2			4									
Cyclone3		4	4									
Stratix		4	4								2	
Stratix2			4									
Stratix3			4								2	
StratixGX		4	4								2	
Stratix2GX			4								2	
Max2		4	4								2	
Max3000a	4	4	4									
Max7000b	4	4	4									
Max7000ae	4	4	4									
Max7000s	4	4	4									
Spartan2		6	2	2								
Spartan2E		6	2	2								
Spartan3		6	2	2								
Spartan3A		4	2	2								
Spartan3ADSP		4	2	2								
Spartan3AN		4	2	2								
Spartan3E		4	2	2								
Spartan3L		4	2	2								
Virtex		6	2	2								
Virtex2		6	2	2								
Virtex2p		6	2	2								
VirtexE		6	2	2								
Virtex4		12	4	4								
Virtex5		4	2	2								
CoolRunner2	4		4									
CoolRunnerXpla3	4		4									
Xc9500	4		4									
Xc9500XL	4		4									
Xc9500XV	4		4									
ProAsicPlus		8										
ProAsic3		8										
ProAsic3E		8										
Fusion		8										
EC		4	4									
ECP		4	4									
ECP2		4	4									
ECP2M		4	4									
SC		4	4									
MACHXO		4										
XP		4	4									
XP2		4	4									

SR4CES

4-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4									
Cyclone		4	4								2	
Cyclone2			4									
Cyclone3		4	4									
Stratix		4	4								2	
Stratix2			4									
Stratix3			4								2	
StratixGX		4	4								2	
Stratix2GX			4								2	
Max2		4	4								2	
Max3000a	4	4	4									
Max7000b	4	4	4									
Max7000ae	4	4	4									
Max7000s	4	4	4									
Spartan2		6	2	2								
Spartan2E		6	2	2								
Spartan3		6	2	2								
Spartan3A		4	2	2								
Spartan3ADSP		4	2	2								
Spartan3AN		4	2	2								
Spartan3E		4	2	2								
Spartan3L		4	2	2								
Virtex		6	2	2								
Virtex2		6	2	2								
Virtex2p		6	2	2								
VirtexE		6	2	2								
Virtex4		12	4	4								
Virtex5		4	2	2								
CoolRunner2	4		4									
CoolRunnerXpla3	4		4									
Xc9500	4		4									
Xc9500XL	4		4									
Xc9500XV	4		4									
ProAsicPlus		8										
ProAsic3		8										
ProAsic3E		8										
Fusion		8										
EC		4	4									
ECP		4	4									
ECP2		4	4									
ECP2M		4	4									
SC		4	4									
MACHXO		4										
XP		4	4									
XP2		4	4									

FPGA Shift Register Resource Usage

SR4CLEB

4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	4									
Cyclone		5	5	4								2	
Cyclone2		5	5	4									
Cyclone3		4	1	4									
Stratix		5	5	4								2	
Stratix2		5	5	4									
Stratix3			1	4								2	
StratixGX		5	5	4								2	
Stratix2GX			5	4								2	
Max2		5	5	4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		7	6	3									
Spartan2E		7	6	3									
Spartan3		7	6	3									
Spartan3A		9	8	3									
Spartan3ADSP		9	8	3									
Spartan3AN		9	8	3									
Spartan3E		9	8	3									
Spartan3L		9	8	3									
Virtex		7	6	3									
Virtex2		7	6	3									
Virtex2p		7	6	3									
VirtexE		7	6	3									
Virtex4		10	9	4									
Virtex5		7	1	3									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		13											
ProAsic3		13											
ProAsic3E		13											
Fusion		13											
EC		10	5	4									
ECP		10	5	4									
ECP2		10	5	4									
ECP2M		10	5	4									
SC		10	5	4									
MACHXO		10	5										
XP		10	5	4									
XP2		10	5	4									

SR4CLEDB

4-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		9	9	4								2	
Cyclone2		9	9	4									
Cyclone3		5	5	4									
Stratix		9	9	4								2	
Stratix2		5	5	4									
Stratix3			5	4								2	
StratixGX		9	9	4								2	
Stratix2GX			5	4								2	
Max2		9	9	4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		14	13	4									
Spartan2E		14	13	4									
Spartan3		14	13	4									
Spartan3A		14	13	4									
Spartan3ADSP		14	13	4									
Spartan3AN		14	13	4									
Spartan3E		18	17	4									
Spartan3L		14	13	4									
Virtex		14	13	4									
Virtex2		14	13	4									
Virtex2p		14	13	4									
VirtexE		14	13	4									
Virtex4		18	17	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		23											
ProAsic3		25											
ProAsic3E		26											
Fusion		25											
EC		10	9	4									
ECP		10	9	4									
ECP2		10	9	4									
ECP2M		10	9	4									
SC		12	11	4									
MACHXO		10	9										
XP		12	10	4									
XP2		10	9	4									

FPGA Shift Register Resource Usage

SR4CLEDS

4-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		9	9	4								2	
Cyclone2		9	9	4									
Cyclone3		5	5	4									
Stratix		9	9	4								2	
Stratix2		5	5	4									
Stratix3			5	4								2	
StratixGX		9	9	4								2	
Stratix2GX			5	4								2	
Max2		9	9	4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		14	13	4									
Spartan2E		14	13	4									
Spartan3		14	13	4									
Spartan3A		14	13	4									
Spartan3ADSP		14	13	4									
Spartan3AN		14	13	4									
Spartan3E		18	17	4									
Spartan3L		14	13	4									
Virtex		14	13	4									
Virtex2		14	13	4									
Virtex2p		14	13	4									
VirtexE		14	13	4									
Virtex4		18	17	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		23											
ProAsic3		25											
ProAsic3E		26											
Fusion		25											
EC		10	9	4									
ECP		10	9	4									
ECP2		10	9	4									
ECP2M		10	9	4									
SC		12	11	4									
MACHXO		10	9										
XP		12	10	4									
XP2		10	9	4									

SR4CLES

4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	4									
Cyclone		5	5	4								2	
Cyclone2		5	5	4									
Cyclone3		4	1	4									
Stratix		5	5	4								2	
Stratix2		5	5	4									
Stratix3			1	4								2	
StratixGX		5	5	4								2	
Stratix2GX			5	4								2	
Max2		5	5	4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		7	6	3									
Spartan2E		7	6	3									
Spartan3		7	6	3									
Spartan3A		9	8	3									
Spartan3ADSP		9	8	3									
Spartan3AN		9	8	3									
Spartan3E		9	8	3									
Spartan3L		9	8	3									
Virtex		7	6	3									
Virtex2		7	6	3									
Virtex2p		7	6	3									
VirtexE		7	6	3									
Virtex4		10	9	4									
Virtex5		5	1	3									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		13											
ProAsic3		13											
ProAsic3E		13											
Fusion		13											
EC		10	5	4									
ECP		10	5	4									
ECP2		10	5	4									
ECP2M		10	5	4									
SC		10	5	4									
MACHXO		10	5										
XP		10	5	4									
XP2		10	5	4									

FPGA Shift Register Resource Usage

SR4REB

4-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		4	4	4									1
Cyclone2		4	4	4									
Cyclone3		5	5	4									
Stratix		4	4	4									1
Stratix2		4	4	4									
Stratix3			5	4									1
StratixGX		4	4	4									1
Stratix2GX			4	4									1
Max2		4	4	4									1
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		6	2	2									
Spartan2E		6	2	2									
Spartan3		6	2	2									
Spartan3A		4	2	2									
Spartan3ADSP		4	2	2									
Spartan3AN		4	2	2									
Spartan3E		4	2	2									
Spartan3L		4	2	2									
Virtex		6	2	2									
Virtex2		6	2	2									
Virtex2p		6	2	2									
VirtexE		6	2	2									
Virtex4		12	4	4									
Virtex5		4	2	2									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		8	4	4									
ECP		8	4	4									
ECP2		4		4									
ECP2M		4		4									
SC		4		4									
MACHXO		8	4										
XP		8	4	4									
XP2		4		4									

SR4RES

4-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		4	4	4									1
Cyclone2		4	4	4									
Cyclone3		5	5	4									
Stratix		4	4	4									1
Stratix2		4	4	4									
Stratix3			5	4									1
StratixGX		4	4	4									1
Stratix2GX			4	4									1
Max2		4	4	4									1
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		6	2	2									
Spartan2E		6	2	2									
Spartan3		6	2	2									
Spartan3A		4	2	2									
Spartan3ADSP		4	2	2									
Spartan3AN		4	2	2									
Spartan3E		4	2	2									
Spartan3L		4	2	2									
Virtex		6	2	2									
Virtex2		6	2	2									
Virtex2p		6	2	2									
VirtexE		6	2	2									
Virtex4		12	4	4									
Virtex5		4	2	2									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		8	4	4									
ECP		8	4	4									
ECP2		4		4									
ECP2M		4		4									
SC		4		4									
MACHXO		8	4										
XP		8	4	4									
XP2		4		4									

FPGA Shift Register Resource Usage

SR4RLEB

4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		8	8	4									1
Cyclone2		8	8	4									
Cyclone3		5	5	4									
Stratix		8	8	4									1
Stratix2		8	8	4									
Stratix3			5	4									1
StratixGX		8	8	4									1
Stratix2GX			4	4									1
Max2		8	8	4									1
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		7	6	3									
Spartan2E		7	6	3									
Spartan3		7	6	3									
Spartan3A		9	8	3									
Spartan3ADSP		9	8	3									
Spartan3AN		9	8	3									
Spartan3E		9	8	3									
Spartan3L		9	8	3									
Virtex		7	6	3									
Virtex2		7	6	3									
Virtex2p		7	6	3									
VirtexE		7	6	3									
Virtex4		10	9	4									
Virtex5		5	1	3									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		17											
ProAsic3		17											
ProAsic3E		17											
Fusion		17											
EC		10	9	4									
ECP		10	9	4									
ECP2		10	5	4									
ECP2M		10	5	4									
SC		10	5	4									
MACHXO		8	8										
XP		10	9	4									
XP2		10	5	4									

SR4RLEDB

4-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		15	15	4									1
Cyclone2		13	13	4									
Cyclone3		9	9	4									
Stratix		15	15	4									1
Stratix2		12	12	4									
Stratix3			5	4									1
StratixGX		15	15	4									1
Stratix2GX			8	4									1
Max2		13	13	4									1
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		14	13	4									
Spartan2E		14	13	4									
Spartan3		14	13	4									
Spartan3A		18	17	4									
Spartan3ADSP		18	17	4									
Spartan3AN		18	17	4									
Spartan3E		18	17	4									
Spartan3L		16	15	4									
Virtex		14	13	4									
Virtex2		14	13	4									
Virtex2p		14	13	4									
VirtexE		14	13	4									
Virtex4		18	17	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		27											
ProAsic3		29											
ProAsic3E		30											
Fusion		29											
EC		16	13	4									
ECP		16	13	4									
ECP2		14	11	4									
ECP2M		14	11	4									
SC		12	11	4									
MACHXO		14	14										
XP		14	14	4									
XP2		14	11	4									

FPGA Shift Register Resource Usage

SR4RLEDS

4-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		5	4									
Cyclone		15	15	4							1	
Cyclone2		13	13	4								
Cyclone3		9	9	4								
Stratix		15	15	4							1	
Stratix2		12	12	4								
Stratix3			5	4							1	
StratixGX		15	15	4							1	
Stratix2GX			8	4							1	
Max2		13	13	4							1	
Max3000a	4	4		4								
Max7000b	4	4		4								
Max7000ae	4	4		4								
Max7000s	4	4		4								
Spartan2		14	13	4								
Spartan2E		14	13	4								
Spartan3		14	13	4								
Spartan3A		18	17	4								
Spartan3ADSP		18	17	4								
Spartan3AN		18	17	4								
Spartan3E		18	17	4								
Spartan3L		16	15	4								
Virtex		14	13	4								
Virtex2		14	13	4								
Virtex2p		14	13	4								
VirtexE		14	13	4								
Virtex4		18	17	4								
Virtex5		4	4	4								
CoolRunner2	4			4								
CoolRunnerXpla3	4			4								
Xc9500	4			4								
Xc9500XL	4			4								
Xc9500XV	4			4								
ProAsicPlus		27										
ProAsic3		29										
ProAsic3E		30										
Fusion		29										
EC		16	13	4								
ECP		16	13	4								
ECP2		14	11	4								
ECP2M		14	11	4								
SC		12	11	4								
MACHXO		14	14									
XP		14	14	4								
XP2		14	11	4								

SR4RLES

4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		8	8	4								1	
Cyclone2		8	8	4									
Cyclone3		5	5	4									
Stratix		8	8	4								1	
Stratix2		8	8	4									
Stratix3			5	4								1	
StratixGX		8	8	4								1	
Stratix2GX			4	4								1	
Max2		8	8	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		7	6	3									
Spartan2E		7	6	3									
Spartan3		7	6	3									
Spartan3A		9	8	3									
Spartan3ADSP		9	8	3									
Spartan3AN		9	8	3									
Spartan3E		9	8	3									
Spartan3L		9	8	3									
Virtex		7	6	3									
Virtex2		7	6	3									
Virtex2p		7	6	3									
VirtexE		7	6	3									
Virtex4		10	9	4									
Virtex5		7	1	3									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		17											
ProAsic3		17											
ProAsic3E		17											
Fusion		17											
EC		10	9	4									
ECP		10	9	4									
ECP2		10	5	4									
ECP2M		10	5	4									
SC		10	5	4									
MACHXO		8	8										
XP		10	9	4									
XP2		10	5	4									

FPGA Shift Register Resource Usage

SR8CEB

8-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8	7	8								2	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8	7	8								2	
Stratix2				8									
Stratix3				8								2	
StratixGX		8	7	8								2	
Stratix2GX				8								2	
Max2		8		8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		14	2	6									
Spartan2E		14	2	6									
Spartan3		14	2	6									
Spartan3A		12	6	6									
Spartan3ADSP		12	6	6									
Spartan3AN		12	6	6									
Spartan3E		12	6	6									
Spartan3L		12	6	6									
Virtex		14	2	6									
Virtex2		14	2	6									
Virtex2p		14	2	6									
VirtexE		14	2	6									
Virtex4		24	8	8									
Virtex5		6	2	6									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		8		8									
ECP		8		8									
ECP2		8		8									
ECP2M		8		8									
SC		8		8									
MACHXO		8											
XP		8		8									
XP2		8		8									

SR8CES

8-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8	7	8									2
Cyclone2				8									
Cyclone3		8		8									
Stratix		8	7	8									2
Stratix2				8									
Stratix3				8									2
StratixGX		8	7	8									2
Stratix2GX				8									2
Max2		8		8									2
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		14	2	6									
Spartan2E		14	2	6									
Spartan3		14	2	6									
Spartan3A		12	6	6									
Spartan3ADSP		12	6	6									
Spartan3AN		12	6	6									
Spartan3E		12	6	6									
Spartan3L		12	6	6									
Virtex		14	2	6									
Virtex2		14	2	6									
Virtex2p		14	2	6									
VirtexE		14	2	6									
Virtex4		24	8	8									
Virtex5		6	2	6									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		8		8									
ECP		8		8									
ECP2		8		8									
ECP2M		8		8									
SC		8		8									
MACHXO		8											
XP		8		8									
XP2		8		8									

FPGA Shift Register Resource Usage

SR8CLEB

8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	8									
Cyclone		9	9	8								2	
Cyclone2		9	9	8									
Cyclone3		8	1	8									
Stratix		9	9	8								2	
Stratix2		9	9	8									
Stratix3			1	8								2	
StratixGX		9	9	8								2	
Stratix2GX			1	8								2	
Max2		9	9	8								2	
Max3000a	9	9		8									
Max7000b	9	9		8									
Max7000ae	9	9		8									
Max7000s	9	9		8									
Spartan2		11	10	7									
Spartan2E		11	10	7									
Spartan3		11	10	7									
Spartan3A		17	16	7									
Spartan3ADSP		17	16	7									
Spartan3AN		17	16	7									
Spartan3E		17	16	7									
Spartan3L		17	16	7									
Virtex		11	10	7									
Virtex2		11	10	7									
Virtex2p		11	10	7									
VirtexE		11	10	7									
Virtex4		18	17	8									
Virtex5		9	1	7									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		25											
ProAsic3		25											
ProAsic3E		25											
Fusion		25											
EC		18	9	8									
ECP		18	9	8									
ECP2		18	9	8									
ECP2M		18	9	8									
SC		18	9	8									
MACHXO		18	9										
XP		18	9	8									
XP2		18	9	8									

SR8CLEDB

8-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9	8									
Cyclone		17	17	8								2	
Cyclone2		17	17	8									
Cyclone3		9	9	8									
Stratix		17	17	8								2	
Stratix2		9	9	8									
Stratix3			9	8								2	
StratixGX		17	17	8								2	
Stratix2GX			9	8								2	
Max2		17	17	8								2	
Max3000a	9	9		8									
Max7000b	9	9		8									
Max7000ae	9	9		8									
Max7000s	9	9		8									
Spartan2		18	17	8									
Spartan2E		18	17	8									
Spartan3		18	17	8									
Spartan3A		26	25	8									
Spartan3ADSP		26	25	8									
Spartan3AN		26	25	8									
Spartan3E		26	25	8									
Spartan3L		26	25	8									
Virtex		18	17	8									
Virtex2		18	17	8									
Virtex2p		18	17	8									
VirtexE		18	17	8									
Virtex4		26	25	8									
Virtex5		6	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		43											
ProAsic3		33											
ProAsic3E		33											
Fusion		33											
EC		18	17	8									
ECP		18	17	8									
ECP2		18	17	8									
ECP2M		18	17	8									
SC		18	17	8									
MACHXO		18	17										
XP		18	17	8									
XP2		18	17	8									

FPGA Shift Register Resource Usage

SR8CLEDS

8-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9	8									
Cyclone		17	17	8								2	
Cyclone2		17	17	8									
Cyclone3		9	9	8									
Stratix		17	17	8								2	
Stratix2		9	9	8									
Stratix3			9	8								2	
StratixGX		17	17	8								2	
Stratix2GX			9	8								2	
Max2		17	17	8								2	
Max3000a	9	9		8									
Max7000b	9	9		8									
Max7000ae	9	9		8									
Max7000s	9	9		8									
Spartan2		18	17	8									
Spartan2E		18	17	8									
Spartan3		18	17	8									
Spartan3A													
Spartan3ADSP		26	25	8									
Spartan3AN		26	25	8									
Spartan3E		26	25	8									
Spartan3L		26	25	8									
Virtex		18	17	8									
Virtex2		18	17	8									
Virtex2p		18	17	8									
VirtexE		18	17	8									
Virtex4		26	25	8									
Virtex5		6	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		43											
ProAsic3		33											
ProAsic3E		33											
Fusion		33											
EC		18	17	8									
ECP		18	17	8									
ECP2		18	17	8									
ECP2M		18	17	8									
SC		18	17	8									
MACHXO		18	17										
XP		18	17	8									
XP2		18	17	8									

SR8CLES

8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	8									
Cyclone		9	9	8								2	
Cyclone2		9	9	8									
Cyclone3		8	1	8									
Stratix		9	9	8								2	
Stratix2		9	9	8									
Stratix3			1	8								2	
StratixGX		9	9	8								2	
Stratix2GX			1	8								2	
Max2		9	9	8								2	
Max3000a	9	9		8									
Max7000b	9	9		8									
Max7000ae	9	9		8									
Max7000s	9	9		8									
Spartan2		11	10	7									
Spartan2E		11	10	7									
Spartan3		11	10	7									
Spartan3A		17	16	7									
Spartan3ADSP		17	16	7									
Spartan3AN		17	16	7									
Spartan3E		17	16	7									
Spartan3L		17	16	7									
Virtex		11	10	7									
Virtex2		11	10	7									
Virtex2p		11	10	7									
VirtexE		11	10	7									
Virtex4		18	17	8									
Virtex5		9	1	7									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		25											
ProAsic3		25											
ProAsic3E		25											
Fusion		25											
EC		18	9	8									
ECP		18	9	8									
ECP2		18	9	8									
ECP2M		18	9	8									
SC		18	9	8									
MACHXO		18	9										
XP		18	9	8									
XP2		18	9	8									

FPGA Shift Register Resource Usage

SR8REB

8-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	8									
Cyclone		9	1	8									1
Cyclone2		1	1	8									
Cyclone3		8	1	8									
Stratix		9	1	8									1
Stratix2		8	8	8									
Stratix3			1	8									1
StratixGX		9	1	8									1
Stratix2GX			1	8									1
Max2		9	1	8									1
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		14	2	6									
Spartan2E		14	2	6									
Spartan3		14	2	6									
Spartan3A		12	6	6									
Spartan3ADSP		12	6	6									
Spartan3AN		12	6	6									
Spartan3E		12	6	6									
Spartan3L		12	6	6									
Virtex		14	2	6									
Virtex2		14	2	6									
Virtex2p		14	2	6									
VirtexE		14	2	6									
Virtex4		24	8	8									
Virtex5		6	2	6									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		8		8									
ECP2M		8		8									
SC		8		8									
MACHXO		16	8										
XP		16	8	8									
XP2		8		8									

SR8RES

8-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	8									
Cyclone		9	1	8									1
Cyclone2		1	1	8									
Cyclone3		8	1	8									
Stratix		9	1	8									1
Stratix2		8	8	8									
Stratix3			1	8									1
StratixGX		9	1	8									1
Stratix2GX			1	8									1
Max2		9	1	8									1
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		14	2	6									
Spartan2E		14	2	6									
Spartan3		14	2	6									
Spartan3A		12	6	6									
Spartan3ADSP		12	6	6									
Spartan3AN		12	6	6									
Spartan3E		12	6	6									
Spartan3L		12	6	6									
Virtex		14	2	6									
Virtex2		14	2	6									
Virtex2p		14	2	6									
VirtexE		14	2	6									
Virtex4		24	8	8									
Virtex5		6	2	6									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		8		8									
ECP2M		8		8									
SC		8		8									
MACHXO		16	8										
XP		16	8	8									
XP2		8		8									

FPGA Shift Register Resource Usage

SR8RLEB

8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	8									
Cyclone		9	9	8									1
Cyclone2		9	9	8									
Cyclone3		8	1	8									
Stratix		9	9	8									1
Stratix2		16	16	8									
Stratix3			1	8									1
StratixGX		9	9	8									1
Stratix2GX			1	8									1
Max2		9	9	8									1
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		11	10	7									
Spartan2E		11	10	7									
Spartan3		11	10	7									
Spartan3A		17	16	7									
Spartan3ADSP		17	16	7									
Spartan3AN		17	16	7									
Spartan3E		17	16	7									
Spartan3L		17	16	7									
Virtex		11	10	7									
Virtex2		11	10	7									
Virtex2p		11	10	7									
VirtexE		11	10	7									
Virtex4		18	17	8									
Virtex5		7	1	7									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		33											
ProAsic3		33											
ProAsic3E		33											
Fusion		33											
EC		16	16	8									
ECP		16	16	8									
ECP2		18	9	8									
ECP2M		18	9	8									
SC		18	9	8									
MACHXO		16	16										
XP		18	17	8									
XP2		18	9	8									

SR8RLEDB

8-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9	8									
Cyclone		17	17	8									1
Cyclone2		17	17	8									
Cyclone3		9	9	8									
Stratix		17	17	8									1
Stratix2		16	16	8									
Stratix3			9	8									1
StratixGX		17	17	8									1
Stratix2GX			9	8									1
Max2		17	17	8									1
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		18	17	8									
Spartan2E		18	17	8									
Spartan3		18	17	8									
Spartan3A		26	25	8									
Spartan3ADSP		26	25	8									
Spartan3AN		26	25	8									
Spartan3E		26	25	8									
Spartan3L		26	25	8									
Virtex		18	17	8									
Virtex2		18	17	8									
Virtex2p		18	17	8									
VirtexE		18	17	8									
Virtex4		26	25	8									
Virtex5		6	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		51											
ProAsic3		41											
ProAsic3E		41											
Fusion		41											
EC		24	24	8									
ECP		24	24	8									
ECP2		18	17	8									
ECP2M		18	17	8									
SC		18	17	8									
MACHXO		32	24										
XP		32	25	8									
XP2		18	17	8									

FPGA Shift Register Resource Usage

SR8RLEDS

8-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9	8									
Cyclone		17	17	8									1
Cyclone2		17	17	8									
Cyclone3		9	9	8									
Stratix		17	17	8									1
Stratix2		16	16	8									
Stratix3			9	8									1
StratixGX		17	17	8									1
Stratix2GX			9	8									1
Max2		17	17	8									1
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		18	17	8									
Spartan2E		18	17	8									
Spartan3		18	17	8									
Spartan3A		26	25	8									
Spartan3ADSP		26	25	8									
Spartan3AN		26	25	8									
Spartan3E		26	25	8									
Spartan3L		26	25	8									
Virtex		18	17	8									
Virtex2		18	17	8									
Virtex2p		18	17	8									
VirtexE		18	17	8									
Virtex4		26	25	8									
Virtex5		6	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		51											
ProAsic3		41											
ProAsic3E		41											
Fusion		41											
EC		24	24	8									
ECP		24	24	8									
ECP2		18	17	8									
ECP2M		18	17	8									
SC		18	17	8									
MACHXO		32	24										
XP		32	25	8									
XP2		18	17	8									

SR8RLES

8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	8									
Cyclone		9	9	8									1
Cyclone2		9	9	8									
Cyclone3		8	1	8									
Stratix		9	9	8									1
Stratix2		16	16	8									
Stratix3			1	8									1
StratixGX		9	9	8									1
Stratix2GX			1	8									1
Max2		9	9	8									1
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		11	10	7									
Spartan2E		11	10	7									
Spartan3		11	10	7									
Spartan3A		17	16	7									
Spartan3ADSP		17	16	7									
Spartan3AN		17	16	7									
Spartan3E		17	16	7									
Spartan3L		17	16	7									
Virtex		11	10	7									
Virtex2		11	10	7									
Virtex2p		11	10	7									
VirtexE		11	10	7									
Virtex4		18	17	8									
Virtex5		9	1	7									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		33											
ProAsic3		33											
ProAsic3E		33											
Fusion		33											
EC		16	16	8									
ECP		16	16	8									
ECP2		18	9	8									
ECP2M		18	9	8									
SC		18	9	8									
MACHXO		16	16										
XP		18	17	8									
XP2		18	9	8									

FPGA Shift Register Resource Usage

SR16CEB

16-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16	15	16								2	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16	15	16								2	
Stratix2				16									
Stratix3				16								2	
StratixGX		16	15	16								2	
Stratix2GX				16								2	
Max2		16		16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		30	2	14									
Spartan2E		30	2	14									
Spartan3		30	2	14									
Spartan3A		28	14	14									
Spartan3ADSP		28	14	14									
Spartan3AN		28	14	14									
Spartan3E		28	14	14									
Spartan3L		28	14	14									
Virtex		30	2	14									
Virtex2		30	2	14									
Virtex2p		30	2	14									
VirtexE		30	2	14									
Virtex4		48	16	16									
Virtex5		10	2	14									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		35											
Fusion		32											
EC		18		16									
ECP		18		16									
ECP2		18		16									
ECP2M		18		16									
SC		18		16									
MACHXO		18											
XP		18		16									
XP2		18		16									

SR16CES

16-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16	15	16								2	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16	15	16								2	
Stratix2				16									
Stratix3				16								2	
StratixGX		16	15	16								2	
Stratix2GX				16								2	
Max2		16		16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		30	2	14									
Spartan2E		30	2	14									
Spartan3		30	2	14									
Spartan3A		28	14	14									
Spartan3ADSP		28	14	14									
Spartan3AN		28	14	14									
Spartan3E		28	14	14									
Spartan3L		28	14	14									
Virtex		30	2	14									
Virtex2		30	2	14									
Virtex2p		30	2	14									
VirtexE		30	2	14									
Virtex4		48	16	16									
Virtex5		10	2	14									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		35											
Fusion		32											
EC		18		16									
ECP		18		16									
ECP2		18		16									
ECP2M		18		16									
SC		18		16									
MACHXO		18											
XP		18		16									
XP2		18		16									

FPGA Shift Register Resource Usage

SR16CLEB

16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		17	17	16								2	
Cyclone2		17	17	16									
Cyclone3		16	1	16									
Stratix		17	17	16								2	
Stratix2		17	17	16									
Stratix3			1	16								2	
StratixGX		17	17	16								2	
Stratix2GX			1	16								2	
Max2		17	17	16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		19	18	15									
Spartan2E		19	18	15									
Spartan3		19	18	15									
Spartan3A		33	32	15									
Spartan3ADSP		33	32	15									
Spartan3AN		33	32	15									
Spartan3E		33	32	15									
Spartan3L		33	32	15									
Virtex		19	18	15									
Virtex2		19	18	15									
Virtex2p		19	18	15									
VirtexE		19	18	15									
Virtex4		34	33	16									
Virtex5		13	1	15									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		49											
ProAsic3		50											
ProAsic3E		53											
Fusion		50											
EC		34	17	16									
ECP		34	17	16									
ECP2		34	17	16									
ECP2M		34	17	16									
SC		34	17	16									
MACHXO		34	17										
XP		34	17	16									
XP2		34	17	16									

SR16CLEDB

16-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17	16									
Cyclone		33	33	16								2	
Cyclone2		33	33	16									
Cyclone3		17	17	16									
Stratix		33	33	16								2	
Stratix2		17	17	16									
Stratix3			17	16								2	
StratixGX		33	33	16								2	
Stratix2GX			17	16								2	
Max2		33	33	16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		34	33	16									
Spartan2E		34	33	16									
Spartan3		34	33	16									
Spartan3A		50	49	16									
Spartan3ADSP		50	49	16									
Spartan3AN		50	49	16									
Spartan3E		50	49	16									
Spartan3L		50	49	16									
Virtex		34	33	16									
Virtex2		34	33	16									
Virtex2p		34	33	16									
VirtexE		34	33	16									
Virtex4		50	49	16									
Virtex5		10	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		83											
ProAsic3		66											
ProAsic3E		70											
Fusion		66											
EC		34	33	16									
ECP		34	33	16									
ECP2		34	33	16									
ECP2M		34	33	16									
SC		34	33	16									
MACHXO		34	33										
XP		34	33	16									
XP2		34	33	16									

FPGA Shift Register Resource Usage

SR16CLEDS

16-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17	16									
Cyclone		33	33	16								2	
Cyclone2		33	33	16									
Cyclone3		17	17	16									
Stratix		33	33	16								2	
Stratix2		17	17	16									
Stratix3			17	16								2	
StratixGX		33	33	16								2	
Stratix2GX			17	16								2	
Max2		33	33	16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		34	33	16									
Spartan2E		34	33	16									
Spartan3		34	33	16									
Spartan3A		50	49	16									
Spartan3ADSP		50	49	16									
Spartan3AN		50	49	16									
Spartan3E		50	49	16									
Spartan3L		50	49	16									
Virtex		34	33	16									
Virtex2		34	33	16									
Virtex2p		34	33	16									
VirtexE		34	33	16									
Virtex4		50	49	16									
Virtex5		10	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		83											
ProAsic3		66											
ProAsic3E		70											
Fusion		66											
EC		34	33	16									
ECP		34	33	16									
ECP2		34	33	16									
ECP2M		34	33	16									
SC		34	33	16									
MACHXO		34	33										
XP		34	33	16									
XP2		34	33	16									

SR16CLES

16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		17	17	16								2	
Cyclone2		17	17	16									
Cyclone3		16	1	16									
Stratix		17	17	16								2	
Stratix2		17	17	16									
Stratix3			1	16								2	
StratixGX		17	17	16								2	
Stratix2GX			1	16								2	
Max2		17	17	16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		19	18	15									
Spartan2E		19	18	15									
Spartan3		19	18	15									
Spartan3A		33	32	15									
Spartan3ADSP		33	32	15									
Spartan3AN		33	32	15									
Spartan3E		33	32	15									
Spartan3L		33	32	15									
Virtex		19	18	15									
Virtex2		19	18	15									
Virtex2p		19	18	15									
VirtexE		19	18	15									
Virtex4		34	33	16									
Virtex5		13	1	15									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		49											
ProAsic3		50											
ProAsic3E		53											
Fusion		50											
EC		34	17	16									
ECP		34	17	16									
ECP2		34	17	16									
ECP2M		34	17	16									
SC		34	17	16									
MACHXO		34	17										
XP		34	17	16									
XP2		34	17	16									

FPGA Shift Register Resource Usage

SR16REB

16-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		17	1	16									1
Cyclone2		1	1	16									
Cyclone3		16	1	16									
Stratix		17	1	16									1
Stratix2		1	1	16									
Stratix3			1	16									1
StratixGX		17	1	16									1
Stratix2GX			1	16									1
Max2		17	1	16									1
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		30	2	14									
Spartan2E		30	2	14									
Spartan3		30	2	14									
Spartan3A		28	14	14									
Spartan3ADSP		28	14	14									
Spartan3AN		28	14	14									
Spartan3E		28	14	14									
Spartan3L		28	14	14									
Virtex		30	2	14									
Virtex2		30	2	14									
Virtex2p		30	2	14									
VirtexE		30	2	14									
Virtex4		48	16	16									
Virtex5		10	2	14									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		48											
ProAsic3		48											
ProAsic3E		51											
Fusion		48											
EC		32	16	16									
ECP		32	16	16									
ECP2		18		16									
ECP2M		18		16									
SC		18		16									
MACHXO		32	16										
XP		32	16	16									
XP2		18		16									

SR16RES

16-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		17	1	16									1
Cyclone2		1	1	16									
Cyclone3		16	1	16									
Stratix		17	1	16									1
Stratix2		1	1	16									
Stratix3			1	16									1
StratixGX		17	1	16									1
Stratix2GX			1	16									1
Max2		17	1	16									1
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		30	2	14									
Spartan2E		30	2	14									
Spartan3		30	2	14									
Spartan3A		28	14	14									
Spartan3ADSP		28	14	14									
Spartan3AN		28	14	14									
Spartan3E		28	14	14									
Spartan3L		28	14	14									
Virtex		30	2	14									
Virtex2		30	2	14									
Virtex2p		30	2	14									
VirtexE		30	2	14									
Virtex4		48	16	16									
Virtex5		10	2	14									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		48											
ProAsic3		48											
ProAsic3E		51											
Fusion		48											
EC		32	16	16									
ECP		32	16	16									
ECP2		18		16									
ECP2M		18		16									
SC		18		16									
MACHXO		32	16										
XP		32	16	16									
XP2		18		16									

FPGA Shift Register Resource Usage

SR16RLEB

16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		17	17	16									1
Cyclone2		17	17	16									
Cyclone3		16	1	16									
Stratix		17	17	16									1
Stratix2		17	17	16									
Stratix3			1	16									1
StratixGX		17	17	16									1
Stratix2GX			1	16									1
Max2		17	17	16									1
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		19	18	15									
Spartan2E		19	18	15									
Spartan3		19	18	15									
Spartan3A		33	32	15									
Spartan3ADSP		33	32	15									
Spartan3AN		33	32	15									
Spartan3E		33	32	15									
Spartan3L		33	32	15									
Virtex		19	18	15									
Virtex2		19	18	15									
Virtex2p		19	18	15									
VirtexE		19	18	15									
Virtex4		34	33	16									
Virtex5		13	1	15									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		65											
ProAsic3		66											
ProAsic3E		69											
Fusion		66											
EC		32	32	16									
ECP		32	32	16									
ECP2		34	17	16									
ECP2M		34	17	16									
SC		34	17	16									
MACHXO		32	32										
XP		34	33	16									
XP2		34	17	16									

SR16RLEDB

16-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17	16									
Cyclone		33	33	16									1
Cyclone2		33	33	16									
Cyclone3		17	17	16									
Stratix		33	33	16									1
Stratix2		17	17	16									
Stratix3			17	16									1
StratixGX		33	33	16									1
Stratix2GX			17	16									1
Max2		33	33	16									1
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		34	33	16									
Spartan2E		34	33	16									
Spartan3		34	33	16									
Spartan3A		50	49	16									
Spartan3ADSP		50	49	16									
Spartan3AN		50	49	16									
Spartan3E		50	49	16									
Spartan3L		50	49	16									
Virtex		34	33	16									
Virtex2		34	33	16									
Virtex2p		34	33	16									
VirtexE		34	33	16									
Virtex4		50	49	16									
Virtex5		10	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		99											
ProAsic3		82											
ProAsic3E		86											
Fusion		82											
EC		48	48	16									
ECP		48	48	16									
ECP2		34	33	16									
ECP2M		34	33	16									
SC		34	33	16									
MACHXO		64	48										
XP		64	49	16									
XP2		34	33	16									

FPGA Shift Register Resource Usage

SR16RLEDS

16-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17	16									
Cyclone		33	33	16									1
Cyclone2		33	33	16									
Cyclone3		17	17	16									
Stratix		33	33	16									1
Stratix2		17	17	16									
Stratix3			17	16									1
StratixGX		33	33	16									1
Stratix2GX			17	16									1
Max2		33	33	16									1
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		34	33	16									
Spartan2E		34	33	16									
Spartan3		34	33	16									
Spartan3A		50	49	16									
Spartan3ADSP		50	49	16									
Spartan3AN		50	49	16									
Spartan3E		50	49	16									
Spartan3L		50	49	16									
Virtex		34	33	16									
Virtex2		34	33	16									
Virtex2p		34	33	16									
VirtexE		34	33	16									
Virtex4		50	49	16									
Virtex5		10	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		99											
ProAsic3		82											
ProAsic3E		86											
Fusion		82											
EC		48	48	16									
ECP		48	48	16									
ECP2		34	33	16									
ECP2M		34	33	16									
SC		34	33	16									
MACHXO		64	48										
XP		64	49	16									
XP2		34	33	16									

SR16RLES

16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		17	17	16									1
Cyclone2		17	17	16									
Cyclone3		16	1	16									
Stratix		17	17	16									1
Stratix2		17	17	16									
Stratix3			1	16									1
StratixGX		17	17	16									1
Stratix2GX			1	16									1
Max2		17	17	16									1
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		19	18	15									
Spartan2E		19	18	15									
Spartan3		19	18	15									
Spartan3A		33	32	15									
Spartan3ADSP		33	32	15									
Spartan3AN		33	32	15									
Spartan3E		33	32	15									
Spartan3L		33	32	15									
Virtex		19	18	15									
Virtex2		19	18	15									
Virtex2p		19	18	15									
VirtexE		19	18	15									
Virtex4		34	33	16									
Virtex5		13	1	15									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		65											
ProAsic3		66											
ProAsic3E		69											
Fusion		66											
EC		32	32	16									
ECP		32	32	16									
ECP2		34	17	16									
ECP2M		34	17	16									
SC		34	17	16									
MACHXO		32	32										
XP		34	33	16									
XP2		34	17	16									

FPGA Shift Register Resource Usage

SR32CEB

32-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				32									
Cyclone		32		32								2	
Cyclone2				32									
Cyclone3		32		32									
Stratix		32		32								2	
Stratix2				32									
Stratix3				32								2	
StratixGX		32		32								2	
Stratix2GX				32								2	
Max2		32		32								2	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		62	2	30									
Spartan2E		62	2	30									
Spartan3		62	2	30									
Spartan3A		60	30	30									
Spartan3ADSP		60	30	30									
Spartan3AN		60	30	30									
Spartan3E		60	30	30									
Spartan3L		60	30	30									
Virtex		62	2	30									
Virtex2		62	2	30									
Virtex2p		62	2	30									
VirtexE		62	2	30									
Virtex4		96	32	32									
Virtex5		18	2	30									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		64											
ProAsic3		70											
ProAsic3E		70											
Fusion		64											
EC		34		32									
ECP		34		32									
ECP2		34		32									
ECP2M		34		32									
SC		34		32									
MACHXO		34											
XP		34		32									
XP2		34		32									

SR32CLEB

32-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	32									
Cyclone		33	33	32									2
Cyclone2		33	33	32									
Cyclone3		32	1	32									
Stratix		33	33	32									2
Stratix2		33	33	32									
Stratix3			2	32									2
StratixGX		33	33	32									2
Stratix2GX			2	32									2
Max2		33	33	32									2
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		35	34	31									
Spartan2E		35	34	31									
Spartan3		35	34	31									
Spartan3A		65	64	31									
Spartan3ADSP		65	64	31									
Spartan3AN		65	64	31									
Spartan3E		65	64	31									
Spartan3L		65	64	31									
Virtex		35	34	31									
Virtex2		35	34	31									
Virtex2p		35	34	31									
VirtexE		35	34	31									
Virtex4		66	65	32									
Virtex5		21	1	31									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		98											
ProAsic3		104											
ProAsic3E		106											
Fusion		99											
EC		66	33	32									
ECP		66	33	32									
ECP2		66	33	32									
ECP2M		66	33	32									
SC		66	33	32									
MACHXO		66	33										
XP		66	33	32									
XP2		66	33	32									

FPGA Shift Register Resource Usage

SR32CLEDB

32-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			33	32									
Cyclone		65	65	32								2	
Cyclone2		65	65	32									
Cyclone3		33	33	32									
Stratix		65	65	32								2	
Stratix2		33	33	32									
Stratix3			34	32								2	
StratixGX		65	65	32								2	
Stratix2GX			34	32								2	
Max2		65	65	32								2	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		66	65	32									
Spartan2E		66	65	32									
Spartan3		66	65	32									
Spartan3A		98	97	32									
Spartan3ADSP		98	97	32									
Spartan3AN		98	97	32									
Spartan3E		98	97	32									
Spartan3L		98	97	32									
Virtex		66	65	32									
Virtex2		66	65	32									
Virtex2p		66	65	32									
VirtexE		66	65	32									
Virtex4		98	97	32									
Virtex5		18	32	32									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		167											
ProAsic3		138											
ProAsic3E		140											
Fusion		131											
EC		66	65	32									
ECP		66	65	32									
ECP2		66	65	32									
ECP2M		66	65	32									
SC		66	65	32									
MACHXO		66	65										
XP		66	65	32									
XP2		66	65	32									

SR32REB

32-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	32									
Cyclone		33	1	32									1
Cyclone2		1	1	32									
Cyclone3		32	1	32									
Stratix		33	1	32									1
Stratix2		1	1	32									
Stratix3			2	32									1
StratixGX		33	1	32									1
Stratix2GX			2	32									1
Max2		33	1	32									1
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		62	2	30									
Spartan2E		62	2	30									
Spartan3		62	2	30									
Spartan3A		60	30	30									
Spartan3ADSP		60	30	30									
Spartan3AN		60	30	30									
Spartan3E		60	30	30									
Spartan3L		60	30	30									
Virtex		62	2	30									
Virtex2		62	2	30									
Virtex2p		62	2	30									
VirtexE		62	2	30									
Virtex4		96	32	32									
Virtex5		18	2	30									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		96											
ProAsic3		102											
ProAsic3E		102											
Fusion		96											
EC		64	32	32									
ECP		64	32	32									
ECP2		34		32									
ECP2M		34		32									
SC		34		32									
MACHXO		64	32										
XP		64	32	32									
XP2		34		32									

FPGA Shift Register Resource Usage

SR32RLEB

32-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	32									
Cyclone		33	33	32									1
Cyclone2		33	33	32									
Cyclone3		32	1	32									
Stratix		33	33	32									1
Stratix2		33	33	32									
Stratix3			2	32									1
StratixGX		33	33	32									1
Stratix2GX			2	32									1
Max2		33	33	32									1
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		35	34	31									
Spartan2E		35	34	31									
Spartan3		35	34	31									
Spartan3A		65	64	31									
Spartan3ADSP		65	64	31									
Spartan3AN		65	64	31									
Spartan3E		65	64	31									
Spartan3L		65	64	31									
Virtex		35	34	31									
Virtex2		35	34	31									
Virtex2p		35	34	31									
VirtexE		35	34	31									
Virtex4		66	65	32									
Virtex5		21	1	31									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		130											
ProAsic3		136											
ProAsic3E		138											
Fusion		131											
EC		64	64	32									
ECP		64	64	32									
ECP2		66	33	32									
ECP2M		66	33	32									
SC		66	33	32									
MACHXO		64	64										
XP		66	65	32									
XP2		66	33	32									

SR32RLEDB

32-Bit Loadable Serial/Parallel-In Parallel-Out Bidirectional Shift Registers with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			33	32									
Cyclone		65	65	32								1	
Cyclone2		65	65	32									
Cyclone3		33	33	32									
Stratix		65	65	32								1	
Stratix2		33	33	32									
Stratix3			34	32								1	
StratixGX		65	65	32								1	
Stratix2GX			34	32								1	
Max2		65	65	32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		66	65	32									
Spartan2E		66	65	32									
Spartan3		66	65	32									
Spartan3A		98	97	32									
Spartan3ADSP		98	97	32									
Spartan3AN		98	97	32									
Spartan3E		98	97	32									
Spartan3L		98	97	32									
Virtex		66	65	32									
Virtex2		66	65	32									
Virtex2p		66	65	32									
VirtexE		66	65	32									
Virtex4		98	97	32									
Virtex5		18	32	32									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		199											
ProAsic3		170											
ProAsic3E		173											
Fusion		163											
EC		96	96	32									
ECP		96	96	32									
ECP2		66	65	32									
ECP2M		66	65	32									
SC		66	65	32									
MACHXO		128	96										
XP		128	97	32									
XP2		66	65	32									

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1

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