FPGA Peripherals Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Peripherals cores.

Core Reference
CR0139 (v1.11) July 17, 2008

Peripherals

The available Peripherals cores are listed as follows:

BT656
CAN
CAN_W
CANB_W
EMAC8
EMAC8_MD
EMAC8_MD_W
EMAC8_W
EMAC32
FPGA_STARTUP8
FPGA_STARTUP16
FPGA_STARTUP32
I2CM
I2CM_W
I2S_W
KEYPADA
KEYPADA_W
LCD16X2A
MAX1104_DAC
PRTIO1X8
PRTIO1X32
PRTIO2X8
PRTIO2X32
PRTIO4X8
PRTIO4X32
PRTIOX1X8
PRTIOX1X32
PRTIOX2X8
PRTIOX2X32
PRTIOX4X8
PRTIOX4X32
PRTO1X8
PRTO1X32
PRTO2X8
PRTO2X32
PRTO4X8
PRTO4X32
PS2
PS2_W
SPI_W
SRL0
SRL0_W
TMR3
TMR3_W
VGA
VGA32
VGA32_16BPP
VGA32_TFT
WB_DUALMASTER
WB_FPU
WB_IDE
WB_INTERCON
WB_IRCODER
WB_IRDEC
WB_LCDCTRL
WB_LCDCTRL_SRAM
WB_MEM_CTRL
WB_MULTIMASTER
WB_OWM
WB_PRTIO
WB_PWM8
WB_PWMX
WB_UART8

BT656

BT656 Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		976	808	335									
Cyclone2			814	336									
Cyclone3		864	864	335									
Stratix		976	809	335									
Stratix2			671	336									
StratixGX		976	809	335									
Spartan2		1329	960	225									
Spartan2E		1317	955	225									
Spartan3		1363	1001	225									
Spartan3A		1,451	1,118	231									
Spartan3E		1377	1014	225									
Spartan3L		1,447	1,115	231									
Virtex		1321	957	225									
Virtex2		1335	992	225									
Virtex2p		1329	987	225									
VirtexE		1321	957	225									
Virtex4		1359	1002	225									
Virtex5		70	70	70									
ProAsicPlus		2625						4					
ProAsic3		4322											
ProAsic3E		4388											
EC		1374	1237	302									
ECP		1374	1237	302									
ECP2		1334	1055	301									
ECP2M		1334	1055	301									
MACHXO		1374	1237										
XP		1486	1265	302									
SC		1574	1422	301									

CAN

CAN Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		1969	1881	833		2						1	
Cyclone2		1957	1953	802		2						1	
Cyclone3		1283	1283	745									
Stratix		1958	1869	833		1						1	
Stratix2		1660	1657	801		2						1	
StratixGX		1958	1870	833		1						1	
Spartan2		1956	1529	753								1	
Spartan2E		1968	1528	751								1	
Spartan3		2067	1640	745								1	
Spartan3A		2,528	2,112	726									
Spartan3E		2789	2322	777									
Spartan3L		2,548	2,146	710									
Virtex		1972	1534	753								1	
Virtex2		1935	1498	752								1	
Virtex2p		1947	1495	752								1	
VirtexE		1966	1528	753								1	
Virtex4		2827	2356	777									
Virtex5		24	24	24									
ProAsic3		4342				1							
ProAsic3E		4232						1					
EC		2008	1850	773			1						
ECP		2008	1850	773			1						
ECP2		1998	1516	753			1						
ECP2M		1998	1516	753			1						
MACHXO		2156	2047				1						
XP		2304	2046	835			1						
SC		2152	1830	798									

CAN_W

CAN Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		2830	2795	1239		1						1	
Cyclone2		2369	2365	1304		1						1	
Cyclone3		1750	1750	1264									
Stratix		2828	2792	1239		1						1	
Stratix2		2411	2408	1303		1						1	
StratixGX		2828	2793	1239		1						1	
Spartan2		2082	1659	749									
Spartan2E		2066	1645	747									
Spartan3		2072	1645	746									
Spartan3A		2,549	2,137	727									
Spartan3E		2821	2336	767									
Spartan3L		2,571	2,167	711									
Virtex		2058	1645	749									
Virtex2		2052	1626	749									
Virtex2p		2064	1630	747									
VirtexE		2050	1637	749									
Virtex4		2833	2358	767									
Virtex5		12	12	12									
ProAsic3		5453											
ProAsic3E		5565											
EC		2112	1944	766									
ECP		2112	1944	766									
ECP2		2082	1610	743									
ECP2M		2082	1610	743									
MACHXO		2250	2146										
XP		2190	1927	788									
SC		2126	1836	801									

CANB_W

CAN Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		2693	2422	1298		1						1	
Cyclone2		2410	2406	1298		1						1	
Stratix		2775	2512	1298		1						1	
Stratix2		1871	1868	1297		1						1	
StratixGX		2775	2513	1298		1						1	
Spartan2		2033	1590	756									
Spartan2E		2035	1590	756									
Spartan3		2081	1630	755									
Spartan3A		2,560	2,146	728									
Spartan3E		2793	2340	761									
Spartan3L		2,568	2,169	712									
Virtex		2035	1591	756									
Virtex2		2069	1615	756									
Virtex2p		2077	1630	756									
VirtexE		2037	1593	756									
Virtex4		2768	2338	748									
Virtex5		5	5	5									
ProAsicPlus		6519											
ProAsic3		5366											
ProAsic3E		5463											
EC		2094	1948	758									
ECP		2094	1948	758									
ECP2		2098	1625	737									
ECP2M		2098	1625	737									
MACHXO		2258	2160										
XP		2210	1941	780									
SC		2148	1841	781									

EMAC8

Ethernet Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		428	388	205		8						8	
Cyclone2		392	386	205		8						9	
Cyclone3		399	399	204									
Stratix		426	387	205		8						9	
Stratix2		329	327	204		8						9	
StratixGX		408	387	205		8						9	
Spartan2		756	627	198		6							
Spartan2E		756	627	198		6							
Spartan3		684	610	192	2								
Spartan3A		700	606	192									
Spartan3E		718	614	204	2								
Spartan3L		684	593	192									
Virtex		756	628	198		6							
Virtex2		684	610	192	2								
Virtex2p		688	610	192	2								
VirtexE		758	628	198		6							
Virtex4		692	616	192	2								
Virtex5		12	12	12									
EC		640	552	205			4						
ECP		640	552	205			4						
MACHXO		540	436				4						
XP		540	436	205			4						

EMAC8_MD

Ethernet MD Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		542	470	292		8						8	
Cyclone2		475	468	292		8						10	
Cyclone3		461	461	291									
Stratix		553	485	292		8						10	
Stratix2		413	410	291		8						10	
StratixGX		528	485	292		8						10	
Spartan2		975	803	283		6							
Spartan2E		975	803	283		6							
Spartan3		923	788	277	2								
Spartan3A		925	784	277									
Spartan3E		949	793	291	2								
Spartan3L		917	769	277									
Virtex		973	803	283		6							
Virtex2		921	788	277	2								
Virtex2p		923	789	277	2								
VirtexE		973	803	283		6							
Virtex4		923	790	277	2								
Virtex5		14	14	14									
EC		780	659	292			4						
ECP		780	659	292			4						
MACHXO		688	530				4						
XP		710	529	292			4						

EMAC8_MD_W

Ethernet MD Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		583	504	304		8						8	
Cyclone2		508	501	304		8						10	
Cyclone3		481	481	303									
Stratix		583	502	304		8						10	
Stratix2		429	426	303		8						10	
StratixGX		550	507	304		8						10	
Spartan2		1024	832	296		6							
Spartan2E		1024	832	296		6							
Spartan3		958	813	288	2								
Spartan3A		968	810	288									
Spartan3E		1009	835	303	2								
Spartan3L		950	794	288									
Virtex		1026	834	296		6							
Virtex2		958	813	288	2								
Virtex2p		956	812	288	2								
VirtexE		1028	834	296		6							
Virtex4		956	813	288	2								
Virtex5		15	15	15									
EC		796	675	304			4						
ECP		796	675	304			4						
XP		736	542	304			4						

EMAC8_W

Ethernet Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		460	409	217		8						8	
Cyclone2		399	393	216		8						9	
Cyclone3		413	413	216									
Stratix		450	401	217		8						9	
Stratix2		345	343	216		8						9	
StratixGX		422	402	217		8						9	
Spartan2		801	661	211		6							
Spartan2E		799	660	211		6							
Spartan3		733	637	203	2								
Spartan3A		743	637	203									
Spartan3E		766	646	216	2								
Spartan3L		731	621	203									
Virtex		801	662	211		6							
Virtex2		735	639	203	2								
Virtex2p		735	642	203	2								
VirtexE		803	663	211		6							
Virtex4		735	638	203	2								
Virtex5		13	13	13									
EC		652	570	217			4						
ECP		652	570	217			4						
MACHXO		576	455				4						
XP		598	454	217			4						

EMAC32

Ethernet Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		1644	1339	727		4						4	
Cyclone2		1311	1305	727		4						8	
Cyclone3		1317	1317	729									
Stratix		1665	1360	727		4						8	
Stratix2		1146	1141	727		4						8	
StratixGX		1408	1357	727		4						8	
Spartan2		2281	1881	643		4							
Spartan2E		2281	1880	643		4							
Spartan3		2266	1875	642	2								
Spartan3A		1,721	1,319	83									
Spartan3E		2479	2006	727	2								
Spartan3L		1,687	1,304	83									
Virtex		2279	1881	643		4							
Virtex2		2272	1890	642	2								
Virtex2p		2260	1882	642	2								
VirtexE		2277	1881	643		4							
Virtex4		2228	1841	624	2				1				
Virtex5		83	83	83									
EC		2014	1778	730			4						
ECP		2014	1778	730			4						
MACHXO		1998	1931				4						
XP		2012	1715	731			4						

FPGA_STARTUP8

FPGA Startup With 8 Bit Delay

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		21	21	9								1	
Cyclone2		25	25	9								1	
Cyclone3		12	12	4									
Stratix		25	25	9								1	
Stratix2		19	19	9								1	
StratixGX		25	25	9								1	
Max2		25	25	9								1	
Max3000a	15	15		9									
Max7000b	15	15		9									
Max7000ae	15	15		9									
Max7000s	15	15		9									
Spartan2		22	12	9								1	
Spartan2E		22	12	9								1	
Spartan3		26	14	9								1	
Spartan3A		20	14	4									
Spartan3E		37	23	9									
Spartan3L		20	14	4									
Virtex		22	12	9								1	
Virtex2		26	14	9								1	
Virtex2p		26	14	9								1	
VirtexE		22	12	9								1	
Virtex4		35	23	9									
CoolRunner2	14			9									
CoolRunnerXpla3	13			9									
Xc9500	12			9									
Xc9500XL	12			9									
Xc9500XV	12			9									
ProAsicPlus		62											
ProAsic3		55											
ProAsic3E		55											
EC		28	26	9									
ECP		28	26	9									
ECP2		28	22	4									
ECP2M		28	22	4									
MACHXO		30	27										
XP		24	22	9									
SC		22	18	4									

FPGA_STARTUP16

FPGA Startup With 16 Bit Delay

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		44	44	17								1	
Cyclone2		49	49	17								1	
Cyclone3		39	39	17									
Stratix		44	44	17								1	
Stratix2		38	38	17								1	
StratixGX		44	44	17								1	
Max2		49	49	17								1	
Max3000a	72	72		17									
Max7000b	72	72		17									
Max7000ae	72	72		17									
Max7000s	72	72		17									
Spartan2		42	24	17								1	
Spartan2E		42	24	17								1	
Spartan3		42	24	17								1	
Spartan3A		61	41	17									
Spartan3E		61	41	17									
Spartan3L		61	41	17									
Virtex		42	24	17								1	
Virtex2		50	27	17								1	
Virtex2p		50	27	17								1	
VirtexE		42	24	17								1	
Virtex4		59	41	17									
CoolRunner2	29			17									
CoolRunnerXpla3	32			17									
Xc9500	42			17									
ProAsicPlus		145											
ProAsic3		127											
ProAsic3E		127											
EC		58	49	17									
ECP		58	49	17									
ECP2		52	49	17									
ECP2M		52	49	17									
MACHXO		60	50										
XP		44	42	17									
SC		58	49	17									

FPGA_STARTUP32

FPGA Startup With 32 Bit Delay

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		86	86	33								1	
Cyclone2		97	97	33								1	
Cyclone3		77	77	33									
Stratix		86	86	33								1	
Stratix2		74	74	33								1	
StratixGX		86	86	33								1	
Max2		97	97	33								1	
Max3000a	130	130		33									
Max7000b	130	130		33									
Max7000ae	130	130		33									
Max7000s	130	130		33									
Spartan2		82	48	33								1	
Spartan2E		82	48	33								1	
Spartan3		90	48	33								1	
Spartan3A		125	81	33									
Spartan3E		125	81	33									
Spartan3L		125	81	33									
Virtex		82	48	33								1	
Virtex2		98	53	33								1	
Virtex2p		98	53	33								1	
VirtexE		82	48	33								1	
Virtex4		123	81	33									
Xc9500XL	106			33									
ProAsicPlus		309											
ProAsic3		269											
ProAsic3E		269											
EC		114	97	33									
ECP		114	97	33									
ECP2		100	97	33									
ECP2M		100	97	33									
XP		92	90	33									
SC		114	97	33									

I2CM

I2C Master

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		173	157	118								1	
Cyclone2		183	183	120								1	
Cyclone3		158	158	120									
Stratix		170	160	118								1	
Stratix2		174	174	120								1	
StratixGX		203	201	120								1	
Spartan2		208	149	98								1	
Spartan2E		208	149	98								1	
Spartan3		206	149	98								1	
Spartan3A		313	265	101									
Spartan3E		354	294	120									
Spartan3L		291	247	85									
Virtex		208	149	98								1	
Virtex2		206	149	98								1	
Virtex2p		206	149	98								1	
VirtexE		208	149	98								1	
Virtex4		348	283	120									
Virtex5		19	19	19									
ProAsicPlus		663											
ProAsic3		589											
ProAsic3E		592											
EC		278	239	121									
ECP		278	239	121									
ECP2		268	185	104									
ECP2M		268	185	104									
MACHXO		338	287										
XP		306	234	120									
SC		292	227	120									

I2CM_W

I2C Master Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		175	158	118								1	
Cyclone2		183	183	121								1	
Cyclone3		160	160	121									
Stratix		177	160	118								1	
Stratix2		178	178	121								1	
StratixGX		211	209	121								1	
Spartan2		210	152	98									
Spartan2E		210	152	98									
Spartan3		210	152	98									
Spartan3A		318	268	102									
Spartan3E		361	300	121									
Spartan3L		294	250	86									
Virtex		208	152	98									
Virtex2		210	152	98									
Virtex2p		210	152	98									
VirtexE		210	152	98									
Virtex4		353	288	121									
Virtex5		19	19	19									
ProAsicPlus		633											
ProAsic3		596											
ProAsic3E		599											
EC		280	242	122									
ECP		280	242	122									
ECP2		272	190	105									
ECP2M		272	190	105									
MACHXO		340	289										
XP		308	238	121									
SC		296	232	121									

I2S_W

I2S Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		99	49	92									
Cyclone2			52	92									
Cyclone3		443	443	181									
Stratix		99	49	92									
Stratix2			21	92									
StratixGX		99	49	92									
Spartan2		130	105	60								1	
Spartan2E		130	105	60								1	
Spartan3		130	105	60								1	
Spartan3A		804	558	112									
Spartan3E		130	105	60								1	
Spartan3L		774	534	112									
Virtex		130	105	60								1	
Virtex2		130	105	60								1	
Virtex2p		130	105	60								1	
VirtexE		130	105	60								1	
Virtex4		130	105	60									
Virtex5		17	17	17									
ProAsicPlus		197											
ProAsic3		184											
ProAsic3E		187											
EC		804	745	129									
ECP		804	745	129									
ECP2		740	635	129									
ECP2M		740	635	129									
MACHXO		810	725										
XP		860	796	136									
SC		828	734	129									

KEYPADA

Keypad

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		35	29	28								6	
Cyclone2		30	27	28								6	
Cyclone3		30	30	28									
Stratix		35	29	28								6	
Stratix2		31	28	28								6	
StratixGX		35	29	28								6	
Max2		34	28	28								4	
Max3000a	32	32		28									
Max7000b	32	32		28									
Max7000ae	32	32		28									
Max7000s	32	32		28									
Spartan2		43	32	23									
Spartan2E		43	32	23									
Spartan3		47	32	23									
Spartan3A		61	50	23									
Spartan3E		72	55	28									
Spartan3L		61	50	23									
Virtex		43	32	23									
Virtex2		47	32	23									
Virtex2p		47	32	23									
VirtexE		43	32	23									
Virtex4		72	55	28									
Virtex5		5	5	5									
CoolRunner2	33			28									
CoolRunnerXpla3	33			28									
Xc9500	33			28									
Xc9500XL	33			28									
Xc9500XV	33			28									
ProAsicPlus		66											
ProAsic3		67											
ProAsic3E		67											
EC		46	31	28									
ECP		46	31	28									
ECP2		56	38	28									
ECP2M		56	38	28									
MACHXO		54	37										
XP		54	35	28									
SC		52	34	28									

KEYPADA_W

Keypad Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		52	41	38								1	
Cyclone2		45	44	38								1	
Cyclone3		39	39	38									
Stratix		52	41	38								1	
Stratix2		42	42	38								1	
StratixGX		52	42	38								1	
Spartan2		59	26	37									
Spartan2E		59	26	37									
Spartan3		61	26	37									
Spartan3A		90	60	32									
Spartan3E		99	66	33									
Spartan3L		90	60	32									
Virtex		59	26	37									
Virtex2		61	26	37									
Virtex2p		61	26	37									
VirtexE		59	26	37									
Virtex4		94	61	32									
Virtex5		1	1	1									
ProAsicPlus		153											
ProAsic3		152											
ProAsic3E		153											
EC		88	76	39									
ECP		88	76	39									
ECP2		72	44	38									
ECP2M		72	44	38									
MACHXO		76	67										
XP		70	62	38									
SC		74	62	38									

LCD16X2A

LCD Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		84	73	49								1	
Cyclone2		79	78	49								1	
Cyclone3		74	74	49									
Stratix		85	74	49								1	
Stratix2		65	65	49								1	
StratixGX		85	75	49								1	
Max2		80	70	49								1	
Max3000a	64	64		49									
Max7000b	64	64		49									
Max7000ae	64	64		49									
Max7000s	64	64		49									
Spartan2		118	84	25								1	
Spartan2E		118	84	25								1	
Spartan3		111	89	24								1	
Spartan3A		114	83	24									
Spartan3E		165	111	49									
Spartan3L		103	78	19									
Virtex		118	84	25								1	
Virtex2		117	91	24								1	
Virtex2p		117	91	24								1	
VirtexE		118	84	25								1	
Virtex4		157	113	49									
Virtex5		25	25	25									
CoolRunner2	49			49									
CoolRunnerXpla3	49			49									
Xc9500	49			49									
Xc9500XL	49			49									
Xc9500XV	49			49									
ProAsicPlus		214											
ProAsic3		212											
ProAsic3E		216											
EC		104	99	49									
ECP		104	99	49									
ECP2		100	73	44									
ECP2M		100	73	44									
MACHXO		116	106										
XP		110	100	49									
SC		110	96	49									

MAX1104_DAC

MAX1104 DAC Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		26	21	22								2	
Cyclone2		22	21	22								2	
Cyclone3		22	22	22									
Stratix		26	21	22								2	
Stratix2		23	22	22								2	
StratixGX		26	22	22								2	
Max2		26	22	22								2	
Max3000a	23	23		22									
Max7000b	23	23		22									
Max7000ae	23	23		22									
Max7000s	23	23		22									
Spartan2		32	22	20								1	
Spartan2E		32	22	20								1	
Spartan3		28	22	20								1	
Spartan3A		46	40	20									
Spartan3E		52	42	22									
Spartan3L		46	40	20									
Virtex		32	22	20								1	
Virtex2		32	22	20								1	
Virtex2p		32	22	20								1	
VirtexE		32	22	20								1	
Virtex4		52	42	22									
Virtex5		2	2	2									
CoolRunner2	22			22									
CoolRunnerXpla3	22			22									
Xc9500	22			22									
Xc9500XL	22			22									
Xc9500XV	22			22									
ProAsicPlus		76											
ProAsic3		69											
ProAsic3E		69											
EC		36	21	22									
ECP		36	21	22									
ECP2		38	22	22									
ECP2M		38	22	22									
MACHXO		40	23										
XP		38	22	22									
SC		34	22	22									

PRTIO1X8

Port IO 1 x 8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		9	1	8								1	
Cyclone2		1	1	8								1	
Cyclone3		8	1	8									
Stratix		9	1	8								1	
Stratix2		8	8	8								1	
StratixGX		9	1	8								1	
Max2		9	1	8								1	
Max3000a	16	16		8									
Max7000b	16	16		8									
Max7000ae	16	16		8									
Max7000s	16	16		8									
Spartan2		8	8	8								1	
Spartan2E		8	8	8								1	
Spartan3		8	8	8								1	
Spartan3A		8	8	8									
Spartan3E		24	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8								1	
Virtex2		8	8	8								1	
Virtex2p		8	8	8								1	
VirtexE		8	8	8								1	
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	16			8									
CoolRunnerXpla3	16			8									
Xc9500	16			8									
Xc9500XL	16			8									
Xc9500XV	16			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		16		8									
ECP2M		16		8									
MACHXO		18	9										
XP		18	9	8									
SC		16	8	8									

PRTIO1X32

Port IO 1 x 32

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		33	1	32								1	
Cyclone2		1	1	32								1	
Cyclone3		32	1	32									
Stratix		33	1	32								1	
Stratix2		1	1	32								1	
StratixGX		33	1	32								1	
Max2		33	1	32								1	
Max3000a	64	64		32									
Max7000b	64	64		32									
Max7000ae	64	64		32									
Max7000s	64	64		32									
Spartan2		32	32	32								1	
Spartan2E		32	32	32								1	
Spartan3		32	32	32								1	
Spartan3A		32	32	32									
Spartan3E		96	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32								1	
Virtex2		32	32	32								1	
Virtex2p		32	32	32								1	
VirtexE		32	32	32								1	
Virtex4		96	32	32									
Virtex5		32	32	32									
CoolRunner2	64			32									
CoolRunnerXpla3	64			32									
Xc9500	64			32									
Xc9500XL	64			32									
Xc9500XV	64			32									
ProAsicPlus		96											
ProAsic3		96											
ProAsic3E		96											
EC		64	32	32									
ECP		64	32	32									
ECP2		64		32									
ECP2M		64		32									
MACHXO		66	33										
XP		66	33	32									
SC		64	32	32									

PRTIO2X8

Port IO 2 x 8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		26	10	16									
Cyclone2		10	10	16								1	
Cyclone3		18	18	16									
Stratix		26	10	16									
Stratix2		10	10	16								1	
StratixGX		26	10	16								1	
Max2		26	10	16								1	
Max3000a	24	24		16									
Max7000b	24	24		16									
Max7000ae	24	24		16									
Max7000s	24	24		16									
Spartan2		26	26	16									
Spartan2E		26	26	16								1	
Spartan3		26	26	16								1	
Spartan3A		26	26	16									
Spartan3E		58	26	16									
Spartan3L		26	26	16									
Virtex		26	26	16								1	
Virtex2		26	26	16								1	
Virtex2p		26	26	16								1	
VirtexE		26	26	16									
Virtex4		58	26	16									
Virtex5		16	16	16									
CoolRunner2	24			16									
CoolRunnerXpla3	24			16									
Xc9500	24			16									
Xc9500XL	24			16									
Xc9500XV	24			16									
ProAsicPlus		58											
ProAsic3		58											
ProAsic3E		58											
EC		48	24	16									
ECP		48	24	16									
ECP2		52	10	16									
ECP2M		52	10	16									
MACHXO		50	27										
XP		50	25	16									
SC		48	24	16									

PRTIO2X32

Port IO 2 x 32

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		98	34	64									
Cyclone2		34	34	64								1	
Cyclone3		66	66	64									
Stratix		98	34	64									
Stratix2		34	34	64								1	
StratixGX		98	34	64								1	
Max2		98	34	64								1	
Max3000a	96	96		64									
Max7000b	96	96		64									
Max7000ae	96	96		64									
Max7000s	96	96		64									
Spartan2		98	98	64									
Spartan2E		98	98	64									
Spartan3		98	98	64								1	
Spartan3A		98	98	64									
Spartan3E		226	98	64									
Spartan3L		98	98	64									
Virtex		98	98	64								1	
Virtex2		98	98	64									
Virtex2p		98	98	64								1	
VirtexE		98	98	64									
Virtex4		226	98	64									
Virtex5		64	64	64									
CoolRunner2	96			64									
CoolRunnerXpla3	96			64									
ProAsicPlus		226											
ProAsic3		228											
ProAsic3E		230											
EC		192	96	64									
ECP		192	96	64									
ECP2		196	34	64									
ECP2M		196	34	64									
MACHXO		194	99										
XP		194	97	64									
SC		192	96	64									

PRTIO4X8

Port IO 4 x 8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		52	20	32									
Cyclone2		20	20	32								1	
Cyclone3		32	28	32									
Stratix		52	20	32									
Stratix2		12	12	32								1	
StratixGX		52	20	32								1	
Max2		52	20	32								1	
Max3000a	40	40		32									
Max7000b	40	40		32									
Max7000ae	40	40		32									
Max7000s	40	40		32									
Spartan2		52	52	32									
Spartan2E		52	52	32									
Spartan3		52	52	32								1	
Spartan3A		52	52	32									
Spartan3E		116	52	32									
Spartan3L		52	52	32									
Virtex		52	52	32									
Virtex2		52	52	32									
Virtex2p		52	52	32									
VirtexE		52	52	32									
Virtex4		116	52	32									
Virtex5		32	32	32									
CoolRunner2	40			32									
CoolRunnerXpla3	40			32									
Xc9500	40			32									
Xc9500XL	40			32									
Xc9500XV	40			32									
ProAsicPlus		136											
ProAsic3		124											
ProAsic3E		124											
EC		80	50	32									
ECP		80	50	32									
ECP2		84	20	32									
ECP2M		84	20	32									
MACHXO		82	53										
XP		82	53	32									
SC		80	52	32									

PRTIO4X32

Port IO 4 x 32

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		196	68	128									
Cyclone2		68	68	128								1	
Cyclone3		128	100	128									
Stratix		196	68	128									
Stratix2		36	36	128								1	
StratixGX		196	68	128								1	
Max2		196	68	128								1	
Max3000a	164	164		128									
Max7000b	164	164		128									
Max7000ae	164	164		128									
Max7000s	164	164		128									
Spartan2		196	196	128									
Spartan2E		196	196	128									
Spartan3		196	196	128								1	
Spartan3A		196	196	128									
Spartan3E		452	196	128									
Spartan3L		196	196	128									
Virtex		196	196	128									
Virtex2		196	196	128									
Virtex2p		196	196	128									
VirtexE		196	196	128									
Virtex4		68	68										
Virtex5		128	128	128									
ProAsicPlus		520											
EC		320	194	128									
ECP		320	194	128									
ECP2		324	68	128									
ECP2M		324	68	128									
MACHXO		322	197										
XP		322	197	128									
SC		320	196	128									

PRTIOX1X8

Port IO Tristate 1 x 8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		18	10	16									
Cyclone2		10	10	16								1	
Cyclone3		16	10	16									
Stratix		18	10	16									
Stratix2		16	16	16								1	
StratixGX		18	10	16								1	
Max2		18	10	16								1	
Max3000a	24	24		16									
Max7000b	24	24		16									
Max7000ae	24	24		16									
Max7000s	24	24		16									
Spartan2		18	18	16									
Spartan2E		18	18	16									
Spartan3		18	18	16								1	
Spartan3A		18	18	16									
Spartan3E		50	18	16									
Spartan3L		18	18	16									
Virtex		18	18	16									
Virtex2		18	18	16									
Virtex2p		18	18	16									
VirtexE		18	18	16									
Virtex4		50	18	16									
Virtex5		16	16	16									
CoolRunner2	24			16									
CoolRunnerXpla3	24			16									
Xc9500	24			16									
Xc9500XL	24			16									
Xc9500XV	24			16									
ProAsicPlus		50											
ProAsic3		50											
ProAsic3E		50											
EC		32	16	16									
ECP		32	16	16									
ECP2		36	2	16									
ECP2M		36	2	16									
MACHXO		34	19										
XP		34	17	16									
SC		32	16	16									

PRTIOX1X32

Port IO Tristate 1 x 32

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		66	34	64									
Cyclone2		34	34	64								1	
Cyclone3		64	2	64									
Stratix		66	34	64									
Stratix2		33	33	64								1	
StratixGX		66	34	64								1	
Max2		66	34	64								1	
Max3000a	96	96		64									
Max7000b	96	96		64									
Max7000ae	96	96		64									
Max7000s	96	96		64									
Spartan2		66	66	64									
Spartan2E		66	66	64									
Spartan3		66	66	64								1	
Spartan3A		66	66	64									
Spartan3E		194	66	64									
Spartan3L		66	66	64									
Virtex		66	66	64									
Virtex2		66	66	64									
Virtex2p		66	66	64									
VirtexE		66	66	64									
Virtex4		194	66	64									
Virtex5		64	64	64									
CoolRunner2	96			64									
CoolRunnerXpla3	96			64									
Xc9500	96			64									
Xc9500XL	96			64									
Xc9500XV	96			64									
ProAsicPlus		194											
ProAsic3		196											
ProAsic3E		198											
EC		128	64	64									
ECP		128	64	64									
ECP2		132	2	64									
ECP2M		132	2	64									
MACHXO		130	67										
XP		130	65	64									
SC		128	64	64									

PRTIOX2X8

Port IO Tristate 2 x 8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		44	28	32									
Cyclone2		28	28	32								1	
Cyclone3		32	28	32									
Stratix		44	28	32									
Stratix2		27	27	32								1	
StratixGX		44	28	32								1	
Max2		44	28	32								1	
Max3000a	40	40		32									
Max7000b	40	40		32									
Max7000ae	40	40		32									
Max7000s	40	40		32									
Spartan2		44	44	32									
Spartan2E		44	44	32									
Spartan3		44	44	32								1	
Spartan3A		44	44	32									
Spartan3E		108	44	32									
Spartan3L		44	44	32									
Virtex		44	44	32									
Virtex2		44	44	32									
Virtex2p		44	44	32									
VirtexE		44	44	32									
Virtex4		108	44	32									
Virtex5		32	32	32									
CoolRunner2	40			32									
CoolRunnerXpla3	40			32									
Xc9500	40			32									
Xc9500XL	40			32									
Xc9500XV	40			32									
ProAsicPlus		109											
ProAsic3		108											
ProAsic3E		109											
EC		80	44	32									
ECP		80	44	32									
ECP2		84	12	32									
ECP2M		84	12	32									
MACHXO		82	45										
XP		82	45	32									
SC		80	44	32									

PRTIOX2X32

Port IO Tristate 2 x 32

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		164	100	128									
Cyclone2		100	100	128								1	
Cyclone3		128	100	128									
Stratix		164	100	128									
Stratix2		99	99	128								1	
StratixGX		164	100	128								1	
Max2		164	100	128								1	
Max3000a	165	165		128									
Max7000b	165	165		128									
Max7000ae	165	165		128									
Max7000s	165	165		128									
Spartan2		164	164	128									
Spartan2E		164	164	128									
Spartan3		164	164	128								1	
Spartan3A		164	164	128									
Spartan3E		420	164	128									
Spartan3L		164	164	128									
Virtex		164	164	128									
Virtex2		164	164	128									
Virtex2p		164	164	128									
VirtexE		164	164	128									
Virtex4		36	36										
Virtex5		128	128	128									
CoolRunner2	160			128									
ProAsicPlus		421											
ProAsic3E		431											
EC		320	164	128									
ECP		320	164	128									
ECP2		324	36	128									
ECP2M		324	36	128									
MACHXO		322	165										
XP		322	165	128									
SC		320	164	128									

PRTIOX4X8

Port IO Tristate 4 x 8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		89	57	64									
Cyclone2		57	57	64								1	
Cyclone3		64	42	64									
Stratix		89	57	64									
Stratix2		48	48	64								1	
StratixGX		89	57	64								1	
Max2		89	57	64								1	
Max3000a	72	72		64									
Max7000b	72	72		64									
Max7000ae	72	72		64									
Max7000s	72	72		64									
Spartan2		88	88	64									
Spartan2E		88	88	64									
Spartan3		88	88	64								1	
Spartan3A		88	88	64									
Spartan3E		216	88	64									
Spartan3L		88	88	64									
Virtex		88	88	64									
Virtex2		88	88	64									
Virtex2p		88	88	64									
VirtexE		88	88	64									
Virtex4		216	88	64									
Virtex5		64	64	64									
CoolRunner2	72			64									
CoolRunnerXpla3	72			64									
Xc9500	72			64									
Xc9500XL	72			64									
Xc9500XV	72			64									
ProAsicPlus		238											
ProAsic3		228											
ProAsic3E		228											
EC		144	86	64									
ECP		144	86	64									
ECP2		152	24	64									
ECP2M		152	24	64									
MACHXO		146	89										
XP		146	89	64									
SC		144	88	64									

PRTIOX4X32

Port IO Tristate 4 x 32

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		329	201	256									
Cyclone2		202	201	256								1	
Cyclone3		256	138	256									
Stratix		329	201	256									
Stratix2		169	168	256								1	
StratixGX		329	201	256								1	
Max2		329	201	256								1	
Max3000a	296	296		256									
Max7000b	296	296		256									
Max7000ae	296	296		256									
Max7000s	296	296		256									
Spartan2		328	328	256									
Spartan2E		328	328	256									
Spartan3		328	328	256								1	
Spartan3A		328	328	256									
Spartan3E		840	328	256									
Spartan3L		328	328	256									
Virtex		328	328	256								1	
Virtex2		328	328	256									
Virtex2p		328	328	256									
VirtexE		328	328	256									
Virtex4		72	72										
Virtex5		256	256	256									
ProAsicPlus		910											
EC		576	332	256									
ECP		576	332	256									
ECP2		584	72	256									
ECP2M		584	72	256									
MACHXO		578	329										
XP		578	329	256									
SC		576	328	256									

PRTO1X8

Port Output 1x8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		9	1	8									
Cyclone2		1	1	8								1	
Cyclone3		8	1	8									
Stratix		9	1	8									
Stratix2		8	8	8								1	
StratixGX		9	1	8								1	
Max2		9	1	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8								1	
Spartan3A		8	8	8									
Spartan3E		24	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		16		8									
ECP2M		16		8									
MACHXO		18	9										
XP		18	9	8									
SC		16	8	8									

PRTO1X32

Port Output 1x32

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		33	1	32									
Cyclone2		1	1	32								1	
Cyclone3		32	1	32									
Stratix		33	1	32									
Stratix2		1	1	32								1	
StratixGX		33	1	32								1	
Max2		33	1	32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32								1	
Spartan3A		32	32	32									
Spartan3E		96	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	32									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		96											
ProAsic3		96											
ProAsic3E		96											
EC		64	32	32									
ECP		64	32	32									
ECP2		64		32									
ECP2M		64		32									
MACHXO		66	33										
XP		66	33	32									
SC		64	32	32									

PRTO2X8

Port Output 2x8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		18	2	16									
Cyclone2		2	2	16								1	
Cyclone3		16	10	16									
Stratix		18	2	16									
Stratix2		2	2	16								1	
StratixGX		18	2	16								1	
Max2		18	2	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		18	18	16									
Spartan2E		18	18	16									
Spartan3		18	18	16								1	
Spartan3A		18	18	16									
Spartan3E		50	18	16									
Spartan3L		18	18	16									
Virtex		18	18	16									
Virtex2		18	18	16									
Virtex2p		18	18	16									
VirtexE		18	18	16									
Virtex4		50	18	16									
Virtex5		16	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		50											
ProAsic3		50											
ProAsic3E		50											
EC		32	16	16									
ECP		32	16	16									
ECP2		36	2	16									
ECP2M		36	2	16									
MACHXO		34	19										
XP		34	17	16									
SC		32	16	16									

PRTO2X32

Port Output 2x32

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		66	2	64									
Cyclone2		2	2	64								1	
Cyclone3		64	34	64									
Stratix		66	2	64									
Stratix2		2	2	64								1	
StratixGX		66	2	64								1	
Max2		66	2	64								1	
Max3000a	64	64		64									
Max7000b	64	64		64									
Max7000ae	64	64		64									
Max7000s	64	64		64									
Spartan2		66	66	64									
Spartan2E		66	66	64									
Spartan3		66	66	64								1	
Spartan3A		66	66	64									
Spartan3E		194	66	64									
Spartan3L		66	66	64									
Virtex		66	66	64									
Virtex2		66	66	64									
Virtex2p		66	66	64									
VirtexE		66	66	64									
Virtex4		194	66	64									
Virtex5		64	64	64									
CoolRunner2	64			64									
CoolRunnerXpla3	64			64									
Xc9500	64			64									
Xc9500XL	64			64									
Xc9500XV	64			64									
ProAsicPlus		194											
ProAsic3		196											
ProAsic3E		198											
EC		128	64	64									
ECP		128	64	64									
ECP2		132	2	64									
ECP2M		132	2	64									
MACHXO		130	67										
XP		130	65	64									
SC		128	64	64									

PRTO4X8

Port Output 4x8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		36	4	32									
Cyclone2		4	4	32								1	
Cyclone3		32	12	32									
Stratix		36	4	32									
Stratix2		4	4	32								1	
StratixGX		36	4	32								1	
Max2		36	4	32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		36	36	32									
Spartan2E		36	36	32									
Spartan3		36	36	32								1	
Spartan3A		36	36	32									
Spartan3E		100	36	32									
Spartan3L		36	36	32									
Virtex		36	36	32									
Virtex2		36	36	32									
Virtex2p		36	36	32									
VirtexE		36	36	32									
Virtex4		100	36	32									
Virtex5		32	32	32									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		102											
ProAsic3		100											
ProAsic3E		100											
EC		64	34	32									
ECP		64	34	32									
ECP2		68	4	32									
ECP2M		68	4	32									
MACHXO		66	37										
XP		66	37	32									
SC		64	36	32									

PRTO4X32

Port Output 4x32

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		132	4	128									
Cyclone2		4	4	128								1	
Cyclone3		128	36	128									
Stratix		132	4	128									
Stratix2		4	4	128								1	
StratixGX		132	4	128								1	
Max2		132	4	128								1	
Max3000a	132	132		128									
Max7000b	132	132		128									
Max7000ae	132	132		128									
Max7000s	132	132		128									
Spartan2		132	132	128									
Spartan2E		132	132	128									
Spartan3		132	132	128								1	
Spartan3A		132	132	128									
Spartan3E		388	132	128									
Spartan3L		132	132	128									
Virtex		132	132	128									
Virtex2		132	132	128									
Virtex2p		132	132	128									
VirtexE		132	132	128									
Virtex4		388	132	128									
Virtex5		128	128	128									
CoolRunner2	128			128									
CoolRunnerXpla3	128			128									
Xc9500	128			128									
Xc9500XL	128			128									
Xc9500XV	128			128									
ProAsicPlus		390											
ProAsic3		392											
ProAsic3E		396											
EC		256	130	128									
ECP		256	130	128									
ECP2		260	4	128									
ECP2M		260	4	128									
MACHXO		258	133										
XP		258	133	128									
SC		256	132	128									

PS2

PS2 Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		159	117	99									
Cyclone2		120	119	100								2	
Cyclone3		101	101	99									
Stratix		157	115	99									
Stratix2		105	105	99								2	
StratixGX		142	116	99								2	
Spartan2		191	100	96									
Spartan2E		187	96	94									
Spartan3		179	103	94								1	
Spartan3A		262	185	94									
Spartan3E		285	195	99									
Spartan3L		265	188	89									
Virtex		191	100	96									
Virtex2		179	102	94									
Virtex2p		179	102	94									
VirtexE		191	100	96									
Virtex4		277	195	99									
Virtex5		5	5	5									
ProAsicPlus		373											
ProAsic3		346											
ProAsic3E		351											
EC		192	157	99									
ECP		192	157	99									
ECP2		180	122	94									
ECP2M		180	122	94									
MACHXO		194	171										
XP		174	121	99									
SC		176	125	99									

PS2_W

PS2 Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		176	126	108									
Cyclone2		132	131	109								2	
Cyclone3		115	115	108									
Stratix		176	126	108									
Stratix2		118	118	108								2	
StratixGX		158	127	108								2	
Spartan2		194	117	96									
Spartan2E		192	117	96									
Spartan3		192	122	96									
Spartan3A		278	199	96									
Spartan3E		306	217	108									
Spartan3L		281	203	91									
Virtex		194	117	96									
Virtex2		190	121	96									
Virtex2p		190	121	96									
VirtexE		194	117	96									
Virtex4		298	216	108									
Virtex5		12	12	12									
ProAsicPlus		417											
ProAsic3		383											
ProAsic3E		385											
EC		220	179	108									
ECP		220	179	108									
ECP2		192	130	103									
ECP2M		192	130	103									
MACHXO		214	192										
XP		198	143	108									
SC		196	145	108									

SPI_W

SPI Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		93	81	70								1	
Cyclone2		93	81	70								1	
Cyclone3		81	81	70									
Stratix		94	81	70								1	
Stratix2		85	64	70								1	
StratixGX		94	81	70								1	
Spartan2		157	116	53									
Spartan2E		157	116	53									
Spartan3		161	117	53									
Spartan3A		161	116	53									
Spartan3E		163	119	53									
Spartan3L		162	120	50									
Virtex		157	116	53									
Virtex2		161	117	53									
Virtex2p		161	117	53									
VirtexE		157	116	53									
Virtex4		165	121	53									
Virtex5		17	17	17									
ProAsicPlus		313											
ProAsic3		293											
ProAsic3E		294											
EC		152	131	70									
ECP		152	131	70									
ECP2		120	76	67									
ECP2M		120	76	67									
MACHXO		152	131										
XP		140	116	70									
SC		152	125	70									

SRL0

Serial 0

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		367	314	155									
Cyclone2		315	315	155								1	
Cyclone3		287	287	155									
Stratix		368	315	155									
Stratix2		279	279	155								1	
StratixGX		325	317	155								1	
Spartan2		360	269	143									
Spartan2E		360	268	143									
Spartan3		370	273	143								1	
Spartan3A		509	413	143									
Spartan3E		535	430	155									
Spartan3L		505	410	143									
Virtex		360	268	143									
Virtex2		366	266	143									
Virtex2p		366	266	143									
VirtexE		360	268	143									
Virtex4		525	421	155									
Virtex5		12	12	12									
ProAsicPlus		858											
ProAsic3		792											
ProAsic3E		796											
EC		418	369	155									
ECP		418	369	155									
ECP2		394	266	155									
ECP2M		394	266	155									
MACHXO		410	367										
XP		414	347	155									
SC		396	337	155									

SRL0_W

Serial 0 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		369	323	155									
Cyclone2		329	329	155								1	
Cyclone3		305	305	155									
Stratix		351	343	155								1	
Stratix2		273	273	155								1	
StratixGX		351	343	155								1	
Spartan2		350	257	143									
Spartan2E		352	257	143									
Spartan3		364	270	143									
Spartan3A		505	410	143									
Spartan3E		529	427	155									
Spartan3L		509	411	143									
Virtex		352	257	143									
Virtex2		364	270	143									
Virtex2p		362	270	143									
VirtexE		352	257	143									
Virtex4		525	416	155									
Virtex5		12	12	12									
ProAsicPlus		813											
ProAsic3		789											
ProAsic3E		792											
EC		398	371	155									
ECP		398	371	155									
ECP2		390	275	155									
ECP2M		390	275	155									
MACHXO		414	367										
XP		406	351	155									
SC		394	333	155									

TMR3

Timer 3

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		190	169	64									
Cyclone2		180	180	64								1	
Cyclone3		166	166	64									
Stratix		186	165	64									
Stratix2		172	172	64								1	
StratixGX		168	166	64								1	
Spartan2		173	157	51									
Spartan2E		173	157	51									
Spartan3		201	185	51								1	
Spartan3A		217	196	51									
Spartan3E		268	218	64									
Spartan3L		215	194	51									
Virtex		173	157	51									
Virtex2		185	162	51									
Virtex2p		185	162	51									
VirtexE		173	157	51									
Virtex4		268	236	64									
Virtex5		13	13	13									
ProAsicPlus		467											
ProAsic3		434											
ProAsic3E		432											
EC		258	249	64									
ECP		258	249	64									
ECP2		218	180	64									
ECP2M		218	180	64									
MACHXO		218	205										
XP		200	183	64									
SC		218	188	64									

TMR3_W

Timer 3 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		188	172	60									
Cyclone2		183	183	60								1	
Cyclone3		168	168	60									
Stratix		187	171	60									
Stratix2		177	177	60								1	
StratixGX		173	171	60								1	
Spartan2		185	166	47									
Spartan2E		185	166	47									
Spartan3		207	189	47									
Spartan3A		213	195	47									
Spartan3E		268	222	60									
Spartan3L		215	196	47									
Virtex		185	166	47									
Virtex2		207	189	47									
Virtex2p		207	188	47									
VirtexE		185	166	47									
Virtex4		264	235	60									
Virtex5		13	13	13									
ProAsicPlus		450											
ProAsic3		399											
ProAsic3E		399											
EC		250	232	60									
ECP		250	232	60									
ECP2		216	183	60									
ECP2M		216	183	60									
MACHXO		216	204										
XP		202	182	60									
SC		236	190	60									

VGA

VGA Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		472	471	58									
Cyclone2		484	483	59								3	
Cyclone3		452	452	58									
Stratix		473	472	58									
Stratix2		418	418	58								3	
StratixGX		473	473	58								3	
Spartan2		479	383	51									
Spartan2E		479	383	51									
Spartan3		523	392	51								1	
Spartan3A		527	430	51									
Spartan3E		510	429	58									
Spartan3L		523	426	51									
Virtex		479	383	51									
Virtex2		497	383	51									
Virtex2p		497	383	51									
VirtexE		479	383	51									
Virtex4		560	444	58									
Virtex5		7	7	7									
ProAsicPlus		1233											
ProAsic3		928											
ProAsic3E		942											
EC		542	529	58									
ECP		542	529	58									
ECP2		540	511	58									
ECP2M		540	511	58									
MACHXO		576	555										
XP		500	466	58									
SC		558	525	60									

VGA32

VGA 32-Bit Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		1096	822	571		6						2	
Cyclone2		889	888	573		6						2	
Cyclone3		772	772	564									
Stratix		1100	826	571		6						2	
Stratix2		606	605	571		6						2	
StratixGX		1123	1006	629		6						2	
Spartan2		2635	1469	507		2							
Spartan2E		2623	1459	507		2							
Spartan3		1485	1102	427	2								
Spartan3A		1,501	1,116	427									
Spartan3E		1634	1223	496	2								
Spartan3L		1,469	1,100	423									
Virtex		2623	1459	507		2							
Virtex2		1485	1102	427	2								
Virtex2p		1481	1100	427	2								
VirtexE		2623	1459	507		2							
Virtex4		1353	976	365	2				3				
Virtex5		69	69	69									
ProAsicPlus		2822						16					
EC		3090	2940	564									
ECP		3090	2940	564									
ECP2		1198	846	501			4						
ECP2M		1198	846	501			4						
MACHXO		2978	2905										
XP		3152	2905	562									
SC		1286	1081	505			4						

VGA32_16BPP

VGA 32-Bit 16 Bpp Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		869	599	522									
Cyclone2			588	522									
Cyclone3		574	574	539									
Stratix		870	600	522									
Stratix2			473	522									
StratixGX		870	600	522									
Spartan2		957	593	85		1							
Spartan2E		955	594	85		1							
Spartan3		911	568	85	1								
Spartan3A		929	566	85									
Spartan3E		913	580	85	1								
Spartan3L		905	553	85									
Virtex		957	593	85		1							
Virtex2		907	566	85	1								
Virtex2p		907	567	85	1								
VirtexE		955	593	85		1							
Virtex4		778	431		1				3				
Virtex5		85	85	85									
ProAsicPlus		2172						8					
ProAsic3		7692											
ProAsic3E		8037											
EC		1422	1156	520									
ECP		1422	1156	520									
ECP2		944	618	484			1						
ECP2M		944	618	484			1						
MACHXO		1422	1156										
XP		1500	1156	520									
SC		938	755	488			1						

VGA32_TFT

VGA 32-Bit TFT Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		972		721		3						2	
Cyclone2			541	721									
Cyclone3		803	733	803									
Stratix		972		721									
Stratix2			457	721									
StratixGX		972		721									
Spartan2		890	509	66		1							
Spartan2E		890	509	66		1							
Spartan3		848	488	68	1								
Spartan3E		852	498	68	1								
Virtex		890	508	66		1							
Virtex2		846	487	68	1								
Virtex2p		846	487	68	1								
VirtexE		892	509	66		1							
Virtex4		760	385		1				3				
ProAsicPlus		2378						8		2			
ProAsic3		8133											
ProAsic3E		8499											
EC		1474	1346	654									
ECP		1474	1346	654									
ECP2		1396	1039	763			1						
ECP2M		1396	1039	763			1						
MACHXO		1474	1346										
XP		1474	1346	654									
SC		1346	1057	764			1						

WB_DUALMASTER

Configurable Wishbone Dual Master

Type : Round Robin Logic Cells/Elements
Address Bus Width : 10-Bits – Range = 1Kb
Data Bus Width : 8-bit

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		39		4								1	
Cyclone2		37		4								1	
Stratix		39		4								1	
Stratix2		37		4								1	
StratixGX		40	40	4								1	
Max3000a	51	51		4									
Max7000b	51	51		4									
Max7000ae	51	51		4									
Max7000s	51	51		4									
Spartan2		38	37	4								1	
Spartan2E		38	37	4								1	
Spartan3		38	37	4								1	
Spartan3E		39	36	3								1	
Virtex		38	37	4								1	
Virtex2		38	37	4								1	
Virtex2p		38	37	4								1	
VirtexE		38	37	4								1	
Virtex4		42	41	4									
CoolRunner2	49			4									
CoolRunnerXpla3	49			4									
Xc9500	49			4									
Xc9500XL	49			4									
Xc9500XV	49			4									
ProAsicPlus		109											
ProAsic3		77											
EC		60	34	3									
ECP		60	34	3									
XP		66	39	4									
MACHXO		66	39	4									

Type : Round Robin
Address Bus Width : 10-Bits – Range = 1Kb
Data Bus Width : 16-bit

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		47		4								1	
Cyclone2		45		4								1	
Stratix		47		4								1	
Stratix2		45		4								1	
StratixGX		48	48	4								1	
Max3000a	75	75		4									
Max7000b	75	75		4									
Max7000ae	75	75		4									
Max7000s	75	75		4									
Spartan2		46	45	4								1	
Spartan2E		46	45	4								1	
Spartan3		46	45	4								1	
Spartan3E		47	44	3								1	
Virtex		46	45	4								1	
Virtex2		46	45	4								1	
Virtex2p		46	45	4								1	
VirtexE		46	45	4								1	
Virtex4		50	49	4									
CoolRunner2	73			4									
CoolRunnerXpla3	73			4									
Xc9500	73			4									
Xc9500XL	73			4									
Xc9500XV	73			4									
ProAsicPlus		133											
ProAsic3		93											
EC		74	42	3									
ECP		74	42	3									
XP		82	47	4									
MACHXO		82	47	4									

FPGA Peripherals Resource Usage

Type : Round Robin
Address Bus Width : 10-Bits – Range = 1Kb
Data Bus Width : 32-bit

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		63		4								1	
Cyclone2		61		4								1	
Stratix		63		4								1	
Stratix2		61		4								1	
StratixGX		64	64	4								1	
Max3000a	123	123		4									
Max7000b	123	123		4									
Max7000ae	123	123		4									
Max7000s	123	123		4									
Spartan2		62	61	4								1	
Spartan2E		62	61	4								1	
Spartan3		62	61	4								1	
Spartan3E		63	60	3								1	
Virtex		62	61	4								1	
Virtex2		62	61	4								1	
Virtex2p		62	61	4								1	
VirtexE		62	61	4								1	
Virtex4		66	65	4									
CoolRunner2	121			4									
CoolRunnerXpla3	121			4									
ProAsicPlus		181											
EC		106	58	3									
ECP		106	58	3									
XP		114	63	4									
MACHXO		114	63	4									

Type : Priority
Priority: m0
Address Bus Width : 10-Bits – Range = 1Kb
Data Bus Width : 8-bit

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		35		2								1	
Cyclone2		31		2								1	
Stratix		34		2								1	
Stratix2		30		2								1	
StratixGX		31	31	2								1	
Max3000a	47	47		2									
Max7000b	47	47		2									
Max7000ae	47	47		2									
Max7000s	47	47		2									
Spartan2		38	35	2								1	
Spartan2E		38	35	2								1	
Spartan3		38	35	2								1	
Spartan3E		32	32	2								1	
Virtex		38	35	2								1	
Virtex2		38	35	2								1	
Virtex2p		38	35	2								1	
VirtexE		38	35	2								1	
Virtex4		40	38	2									
CoolRunner2	47			2									
CoolRunnerXpla3	47			2									
Xc9500	47			2									
Xc9500XL	47			2									
Xc9500XV	47			2									
ProAsicPlus		93											
ProAsic3		62											
EC		58	31	2									
ECP		58	31	2									
XP		58	32	2									
MACHXO		58	32	2									

FPGA Peripherals Resource Usage

Type : Priority
Priority: m0
Address Bus Width : 10-Bits – Range = 1Kb
Data Bus Width : 16-bit

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		43		2								1	
Cyclone2		39		2								1	
Stratix		42		2								1	
Stratix2		38		2								1	
StratixGX		39	39	2								1	
Max3000a	71	71		2									
Max7000b	71	71		2									
Max7000ae	71	71		2									
Max7000s	71	71		2									
Spartan2		46	43	2								1	
Spartan2E		46	43	2								1	
Spartan3		46	43	2								1	
Spartan3E		40	40	2								1	
Virtex		46	43	2								1	
Virtex2		46	43	2								1	
Virtex2p		46	43	2								1	
VirtexE		46	43	2								1	
Virtex4		48	46	2									
CoolRunner2	71			2									
CoolRunnerXpla3	71			2									
Xc9500	71			2									
Xc9500XL	71			2									
Xc9500XV	71			2									
ProAsicPlus		117											
ProAsic3		78											
EC		74	39	2									
ECP		74	39	2									
XP		74	40	2									
MACHXO		74	40	2									

Type : Priority
Priority: m0
Address Bus Width : 10-Bits – Range = 1Kb
Data Bus Width : 32-bit

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		59		2								1	
Cyclone2		55		2								1	
Stratix		58		2								1	
Stratix2		54		2								1	
StratixGX		55	55	2								1	
Max3000a	119	119		2									
Max7000b	119	119		2									
Max7000ae	119	119		2									
Max7000s	119	119		2									
Spartan2		62	59	2								1	
Spartan2E		62	59	2								1	
Spartan3		62	59	2								1	
Spartan3E		58	57	2								1	
Virtex		62	59	2								1	
Virtex2		62	59	2								1	
Virtex2p		62	59	2								1	
VirtexE		62	59	2								1	
Virtex4		64	62	2									
CoolRunner2	119			2									
CoolRunnerXpla3	119			2									
ProAsicPlus		165											
EC		106	55	2									
ECP		106	55	2									
XP		106	56	2									
MACHXO		106	56	2									

WB_FPU

IEEE754 single precision floating point unit

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		4875		709									
Cyclone2		3366	3366	709					14				
Cyclone3		2974	2974	706					14				
Spartan2		5,497	4,957	797									
Spartan2E		5,544	4,980	802									
Spartan3		4,202	3,725	702									
Spartan3A		4,692	4,140	746					3				
Spartan3L		4,149	3,680	693									
Virtex		5,463	4,887	773									
Virtex2		3,741	3,438	673									
Virtex2p		3,868	3,434	672									
VirtexE		5,388	4,836	760									
Virtex4		4,028	3,525	672									
Virtex5		38	38	38									
EC		7024	5929	741									
ECP		4008	3472	722					2				
ECP2		3820	3316	708									
ECP2M		3820	3316	708									
SC		7678	6271	725									
XP		6862	5824	745									
MACHXO		5960	5824										

WB_IDE

IDE Core Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone2		221	221	150									
Cyclone3		167	167	150									
Spartan2		274	238	54									
Spartan2E		264	225	54									
Spartan3		234	222	54									
Spartan3A		234	225	54									
Spartan3L		232	222	54									
Virtex		262	225	54									
Virtex2		234	222	54									
Virtex2p		232	223	54									
VirtexE		260	224	54									
Virtex4		226	221	54									
EC		394	242	166									
ECP		394	242	166									
ECP2		396	215	166									
ECP2M		396	215	166									
SC		364	241	150									
XP		394	242	166									
MACHXO		386	242										

WB_INTERCON

Configurable Wishbone Interconnect

Type: Peripheral Logic Cells/Elements
Address Bus Mode: Word Addressing – ADR_0(0) <= ADR_I(1 or 2)
Decode Addressing: 8
Address Bus Width : 0 Bits – Range = 1
Data Bus Width : 32-bits
Unused Interrupts: Add SPARE INT input pin
Master Address Size: 24-Bit (Peripheral I/O)

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		38											
Cyclone2		38											
Stratix		38											
Stratix2		37											
StratixGX		38	38										
Max3000a	106	106											
Max7000b	106	106											
Max7000ae	106	106											
Max7000s	106	106											
Spartan2		40	38										
Spartan2E		40	38										
Spartan3		40	38										
Spartan3E		38	38										
Virtex		40	38										
Virtex2		40	38										
Virtex2p		40	38										
VirtexE		40	38										
Virtex4		40	38										
CoolRunner2	106												
CoolRunnerXpla3	106												
ProAsicPlus		40											
ProAsic3		40											
EC		38	38										
ECP		38	38										
XP		38	38										
MACHXO		38	38										

Type: ROM
Address Bus Mode: Word Addressing – ADR_0(0) <= ADR_I(1 or 2)
Decode Addressing: 8
Address Bus Width : 0 Bits – Range = 1
Data Bus Width : 8-bits
Unused Interrupts: Add SPARE INT input pin
Master Address Size: 32-Bit (Memory)

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		38											
Cyclone2		38											
Stratix		39											
Stratix2		37											
StratixGX		38	38										
Max3000a	82	82											
Max7000b	82	82											
Max7000ae	82	82											
Max7000s	82	82											
Spartan2		40	38										
Spartan2E		40	38										
Spartan3		40	38										
Spartan3E		38	38										
Virtex		40	38										
Virtex2		40	38										
Virtex2p		40	38										
VirtexE		40	38										
Virtex4		40	38										
CoolRunner2	82												
CoolRunnerXpla3	82												
Xc9500	82												
Xc9500XL	82												
Xc9500XV	82												
ProAsicPlus		104											
ProAsic3		47											
EC		38	38										
ECP		38	38										
XP		38	38										
MACHXO		38	38										

FPGA Peripherals Resource Usage

Type: RAM - Volatile
Address Bus Mode: Word Addressing – ADR_0(0) <= ADR_I(1 or 2)
Decode Addressing: 8
Address Bus Width : 0 Bits – Range = 1
Data Bus Width : 8-bits
Unused Interrupts: Add SPARE INT input pin
Master Address Size: 32-Bit (Memory)

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		38											
Cyclone2		38											
Stratix		38											
Stratix2		37											
StratixGX		38	38										
Max3000a	106	106											
Max7000b	106	106											
Max7000ae	106	106											
Max7000s	106	106											
Spartan2		40	38										
Spartan2E		40	38										
Spartan3		40	38										
Spartan3E		38	38										
Virtex		40	38										
Virtex2		40	38										
Virtex2p		40	38										
VirtexE		40	38										
Virtex4		40	38										
CoolRunner2	106												
CoolRunnerXpla3	106												
ProAsicPlus		40											
ProAsic3		47											
EC		38	38										
ECP		38	38										
XP		38	38										
MACHXO		38	38										

Type: RAM - Non-Volatile
Address Bus Mode: Word Addressing – ADR_0(0) <= ADR_I(1 or 2)
Decode Addressing: 8
Address Bus Width : 0 Bits – Range = 1
Data Bus Width : 8-bits
Unused Interrupts: Add SPARE INT input pin
Master Address Size: 32-Bit (Memory)

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		38											
Cyclone2		38											
Stratix		38											
Stratix2		37											
StratixGX		38	38										
Max3000a	106	106											
Max7000b	106	106											
Max7000ae	106	106											
Max7000s	106	106											
Spartan2		40	38										
Spartan2E		40	38										
Spartan3		40	38										
Spartan3E		38	38										
Virtex		40	38										
Virtex2		40	38										
Virtex2p		40	38										
VirtexE		40	38										
Virtex4		40	38										
CoolRunner2	106												
CoolRunnerXpla3	106												
ProAsicPlus		40											
ProAsic3		47											
EC		38	38										
ECP		38	38										
XP		38	38										
MACHXO		38	38										

WB_IRCODER

IR Coder Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		402		283								2	
Cyclone2		409	361	283								2	
Cyclone3		407	362	282								2	
Stratix		400		283								2	
StratixGX		400		283								2	
Stratix2			300	283								2	
Spartan2		600	522	218									
Spartan2E		602	523	218									
Spartan3		602	523	218									
Spartan3A		602	523	218									
Virtex		604	524	218									
Virtex2		604	524	218									
Virtex2p		604	524	218									
VirtexE		604	524	218									
Virtex4		602	523	218									
Virtex5		677	256	218									
ProAsicPlus		1182								2			
ProAsic3		974											
ProAsic3E		974											
EC		494	350	283									
ECP		494	350	283									
ECP2		506	363	283									
ECP2M		506	363	283									
SC		528	426	284									
XP		494	350	283									
MACHXO		452	350										

WB_IRDEC

IR Decoder Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		458		208									
Cyclone2		354	354	208									
Cyclone3		321	321	208									
Spartan2		611	498	159									
Spartan2E		617	503	159									
Spartan3		597	486	159									
Spartan3A		601	488	159									
Virtex		613	497	159									
Virtex2		607	494	159									
Virtex2p		605	494	159									
VirtexE		609	497	159									
Virtex4		601	490	159									
Virtex5		49	49	49									
ProAsicPlus		986								2			
ProAsic3		884											
ProAsic3E		884											
EC		484	354	208									
ECP		484	354	208									
ECP2		524	378	208									
ECP2M		524	378	208									
SC		548	419	208									
XP		484	354	208									
MACHXO		466	354										

WB_LCDCTRL

LCD Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		31	30	13								1	
Cyclone2		22	7	13								1	
Cyclone3		35	35	13									
Stratix		31	30	13								1	
Stratix2		25	1	13								1	
StratixGX		35	35	13								1	
Spartan2		32	23	13									
Spartan2E		32	23	13									
Spartan3		32	23	13									
Spartan3A		43	32	13									
Spartan3E		41	33	13								1	
Spartan3L		43	32	13									
Virtex		32	23	13									
Virtex2		32	23	13									
Virtex2p		32	23	13									
VirtexE		32	23	13									
Virtex4		41	40	13									
ProAsicPlus		67											
ProAsic3E		56											
EC		24	23	14									
ECP		24	23	14									
ECP2		42	39	13									
ECP2M		42	39	13									
MACHXO		42	39										
XP		42	39	13									
SC		44	39	13									

WB_LCDCTRL_SRAM

LCD Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		78	32	13								1	
Cyclone2		34	7	13								1	
Cyclone3		45	45	13									
Stratix		80	32	13								1	
Stratix2		36	1	13								1	
StratixGX		45	45	13								1	
Spartan2		82	79	13								2	
Spartan2E		82	79	13								2	
Spartan3		82	79	13								2	
Spartan3A		53	43	13									
Spartan3E		53	45	13								1	
Spartan3L		53	43	13									
Virtex		82	79	13								2	
Virtex2		82	79	13								2	
Virtex2p		82	79	13								2	
VirtexE		82	79	13								2	
Virtex4		57	55	13									
ProAsicPlus		140											
ProAsic3E		71											
EC		44	33	14									
ECP		44	33	14									
ECP2		88	65	13									
ECP2M		88	65	13									
MACHXO		84	65										
XP		88	65	13									
SC		94	65	13									

WB_MEM_CTRL

Configurable Memory Controller

Memory Type: Asynchron Logic Cells/Elements
Size of Static RAM array: 1 Kb (256 x 32-bit)
Memory Layout: 1 x 16-bit Wide Devices

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		58		25									
Cyclone2			42	25									
Stratix		58		25									
Stratix2			35	25									
StratixGX		58		25									
Spartan2		61	55	9								1	
Spartan2E		61	55	9								1	
Spartan3		61	55	9								1	
Spartan3E		61	55	9								1	
Virtex		61	55	9								1	
Virtex2		61	55	9								1	
Virtex2p		61	55	9								1	
VirtexE		61	55	9								1	
Virtex4		61	55	9									
ProAsicPlus		123								2			
ProAsic3		108											
ProAsic3E		108											
EC		88	54	25									
ECP		88	54	25									
XP		88	54	25									
MACHXO		88	54	25									

Memory Type: Asynchronous SRAM
Size of Static RAM array: 1 Kb (256 x 32-bit)
Memory Layout: 1 x 8-bit Wide Devices

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		85		43									
Cyclone2			61	43									
Stratix		85		43									
Stratix2			48	43									
StratixGX		85		43									
Spartan2		79	72	19								1	
Spartan2E		79	72	19								1	
Spartan3		79	72	19								1	
Spartan3E		79	72	19								1	
Virtex		79	72	19								1	
Virtex2		79	72	19								1	
Virtex2p		79	72	19								1	
VirtexE		79	72	19								1	
Virtex4		79	72	19									
ProAsicPlus		215								2			
ProAsic3		176											
ProAsic3E		176											
EC		138	74	43									
ECP		138	74	43									
XP		138	74	43									
MACHXO		138	74	43									

Memory Type: Asynchronous SRAM
Size of Static RAM array: 1 Kb (256 x 32-bit)
Memory Layout: 2 x 16-bit Wide Devices

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		22		4									
Cyclone2			22	4									
Stratix		22		4									
Stratix2			13	4									
StratixGX		22		4									
Spartan2		36	32	4								1	
Spartan2E		36	32	4								1	
Spartan3		36	32	4								1	
Spartan3E		36	32	4								1	
Virtex		36	32	4								1	
Virtex2		36	32	4								1	
Virtex2p		36	32	4								1	
VirtexE		36	32	4								1	
Virtex4		38	33	4									
ProAsicPlus		48								2			
ProAsic3		47											
ProAsic3E		47											
EC		62	58	4									
ECP		62	58	4									
XP		62	58	4									
MACHXO		62	58	4									

Memory Type: Asynchronous SRAM
Size of Static RAM array: 1 Kb (256 x 32-bit)
Memory Layout: 2 x 8-bit Wide Devices

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		59		25									
Cyclone2			43	25									
Stratix		59		25									
Stratix2			35	25									
StratixGX		59		25									
Spartan2		59	54	9								1	
Spartan2E		59	54	9								1	
Spartan3		59	54	9								1	
Spartan3E		59	54	9								1	
Virtex		59	54	9								1	
Virtex2		59	54	9								1	
Virtex2p		59	54	9								1	
VirtexE		59	54	9								1	
Virtex4		61	55	9									
ProAsicPlus		120								2			
ProAsic3		106											
ProAsic3E		106											
EC		88	53	25									
ECP		88	53	25									
XP		88	53	25									
MACHXO		88	53	25									

FPGA Peripherals Resource Usage

Memory Type: Block RAM
Size of Block RAM array: 1 Kb (256 x 32-bit)

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		2		1									
Cyclone2			2	1									
Stratix		2		1									
Stratix2			2	1									
StratixGX		2		1									
Spartan2		3	2	1								1	
Spartan2E		3	2	1								1	
Spartan3		3	2	1								1	
Spartan3E		3	2	1								1	
Virtex		3	2	1								1	
Virtex2		3	2	1								1	
Virtex2p		3	2	1								1	
VirtexE		3	2	1								1	
Virtex4		3	2	1									
ProAsicPlus		3								2			
ProAsic3E		3											
EC		2	1	1									
ECP		2	1	1									
XP		2	1	1									
MACHXO		2	1	1									

Memory Type: Synchronous DRAM
Size of SDRAM memory: 16MB (4M x 32-bit)
Memory Layout: 1 x 32-bit Wide Devices
Configuration: PC100

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		403		316									
Cyclone2			196	316									
Stratix		402		316									
Stratix2			163	316									
StratixGX		400		316									
Spartan2		726	554	270									
Spartan2E		699	535	259									
Spartan3		694	532	258									
Spartan3E		688	530	254									
Virtex		758	567	274									
Virtex2		649	496	245									
Virtex2p		654	501	244									
VirtexE		709	530	265									
Virtex4		642	491	244									
ProAsicPlus		907								2			
ProAsic3E		769											

Memory Type: Synchronous DRAM
Size of SDRAM memory: 16MB (4M x 32-bit)
Memory Layout: 1 x 32-bit Wide Devices
Configuration: PC66

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		403		316									
Cyclone2			196	316									
Stratix		402		316									
Stratix2			163	316									
StratixGX		400		316									
Spartan2		726	554	270									
Spartan2E		699	535	259									
Spartan3		694	532	258									
Spartan3E		688	530	254									
Virtex		758	567	274									
Virtex2		649	496	245									
Virtex2p		654	501	244									
VirtexE		709	530	265									
Virtex4		642	491	244									
ProAsicPlus		907								2			
ProAsic3E		769											

Memory Type: Synchronous DRAM
Size of SDRAM memory: 32MB (4M x 32-bit)
Memory Layout: 1 x 32-bit Wide Devices
Configuration: PC100

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		409		323									
Cyclone2			204	323									
Stratix		410		323									
Stratix2			169	323									
StratixGX		409		323									
Spartan2		734	560	278									
Spartan2E		733	562	273									
Spartan3		697	537	269									
Spartan3E		715	551	263									
Virtex		732	552	272									
Virtex2		663	510	251									
Virtex2p		667	517	251									
VirtexE		730	551	276									
Virtex4		658	507	250									
ProAsicPlus		926								2			
ProAsic3E		780											

FPGA Peripherals Resource Usage

Memory Type: Synchronous DRAM
Size of SDRAM memory: 32MB (4M x 32-bit)
Memory Layout: 1 x 32-bit Wide Devices
Configuration: PC66

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		409		323									
Cyclone2			204	323									
Stratix		410		323									
Stratix2			169	323									
StratixGX		409		323									
Spartan2		734	560	278									
Spartan2E		733	562	273									
Spartan3		697	537	269									
Spartan3E		715	551	263									
Virtex		732	552	272									
Virtex2		663	510	251									
Virtex2p		667	517	251									
VirtexE		730	551	276									
Virtex4		658	507	250									
ProAsicPlus		926								2			
ProAsic3E		780											

Memory Type: Synchronous DRAM
Size of SDRAM memory: 64MB (4M x 32-bit)
Memory Layout: 1 x 32-bit Wide Devices
Configuration: PC100

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		428		330									
Cyclone2			201	330									
Stratix		428		330									
Stratix2			168	330									
StratixGX		425		330									
Spartan2		768	579	282									
Spartan2E		736	559	270									
Spartan3		778	587	284									
Spartan3E		735	562	267									
Virtex		742	554	278									
Virtex2		674	514	256									
Virtex2p		674	514	256									
VirtexE		747	562	275									
Virtex4		686	523	256									
ProAsicPlus		929								2			
ProAsic3E		782											

Memory Type: Synchronous DRAM
Size of SDRAM memory: 64MB (4M x 32-bit)
Memory Layout: 1 x 32-bit Wide Devices
Configuration: PC66

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		428		330									
Cyclone2			201	330									
Stratix		428		330									
Stratix2			168	330									
StratixGX		425		330									
Spartan2		768	579	282									
Spartan2E		736	559	270									
Spartan3		778	587	284									
Spartan3E		735	562	267									
Virtex		742	554	278									
Virtex2		674	514	256									
Virtex2p		674	514	256									
VirtexE		747	562	275									
Virtex4		686	523	256									
ProAsicPlus		929								2			
ProAsic3E		782											

WB_MULTIMASTER

Configurable Wishbone Multi Master

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		76		1									
Cyclone2			75	1									
Cyclone3		75	75	1									
Stratix		75		1									
Stratix2			74	1									
StratixGX		75		1									
Spartan2		80	80	2								1	
Spartan2E		80	80	2								1	
Spartan3		82	80	2								1	
Spartan3A		82	80	2									
Spartan3E		82	80	2								1	
Spartan3L		82	80	2									
Virtex		80	80	2								1	
Virtex2		82	80	2								1	
Virtex2p		82	80	2								1	
VirtexE		80	80	2								1	
Virtex4		82	80	2									
ProAsicPlus		227											
ProAsic3		155											
ProAsic3E		155											
EC		148	77	2									
ECP		148	77	2									
ECP2		150	77	2									
ECP2M		150	77	2									
MACHXO		148	77										
XP		148	77	2									
SC		148	76	2									

WB_OWM

Wishbone One Wire Master Controller

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		498		178									
Cyclone2		415	415	178									
Cyclone3		438	438	178									
Spartan2		785	645	177									
Spartan2E		732	602	168									
Spartan3		692	592	168									
Spartan3A		700	600	168									
Virtex		703	596	173									
Virtex2		678	583	168									
Virtex2p		674	581	168									
VirtexE		700	597	172									
Virtex4		686	588	168									
Virtex5		10	10	10									
ProAsicPlus		1001								2			
ProAsic3		853											
ProAsic3E		853											
EC		576	446	178									
ECP		576	446	178									
ECP2		552	427	178									
ECP2M		552	427	178									
SC		634	508	180									
XP		576	446	178									
MACHXO		546	446										

WB_PRTIO

Configurable Port Wishbone

Port IO 1 x 8 Wishbone Logic Cells/Elements

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		10	2	8								1	
Cyclone2		2	2	8								1	
Stratix		10	2	8								1	
Stratix2		9	9	8								1	
StratixGX		10	2	8								1	
Spartan2		10	10	8									
Spartan2E		10	10	8									
Spartan3		10	10	8									
Spartan3E		18	10	8									
Virtex		10	10	8									
Virtex2		10	10	8									
Virtex2p		10	10	8									
VirtexE		10	10	8									
Virtex4		26	10	8									
ProAsicPlus		26											
ProAsic3		26											
ProAsic3E		26											
EC		16	9	8									
ECP		16	9	8									
XP		20	11	8									
MACHXO		20	11	8									

Port IO 1 x 32 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		34	2	32								1	
Cyclone2		2	2	32								1	
Stratix		34	2	32								1	
Stratix2		2	2	32								1	
StratixGX		34	2	32								1	
Spartan2		34	34	32									
Spartan2E		34	34	32									
Spartan3		34	34	32									
Spartan3E		66	34	32									
Virtex		34	34	32									
Virtex2		34	34	32									
Virtex2p		34	34	32									
VirtexE		34	34	32									
Virtex4		98	34	32									
ProAsicPlus		98											
ProAsic3		99											
ProAsic3E		100											
EC		64	33	32									
ECP		64	33	32									
XP		68	35	32									
MACHXO		68	35	32									

Port IO 2 x 8 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		27	11	16									
Cyclone2		11	11	16								1	
Stratix		27	11	16								1	
Stratix2		11	11	16								1	
StratixGX		27	11	16								1	
Spartan2		28	27	16									
Spartan2E		28	27	16									
Spartan3		28	27	16									
Spartan3E		44	27	16									
Virtex		28	27	16									
Virtex2		28	27	16									
Virtex2p		28	27	16									
VirtexE		28	27	16									
Virtex4		60	27	16									
ProAsicPlus		60											
ProAsic3		59											
ProAsic3E		59											
EC		50	26	16									
ECP		50	26	16									
XP		52	28	16									
MACHXO		52	28	16									

Port IO 2 x 32 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		99	35	64									
Cyclone2		35	35	64								1	
Stratix		99	35	64									
Stratix2		35	35	64								1	
StratixGX		99	35	64								1	
Spartan2		100	99	64									
Spartan2E		100	99	64									
Spartan3		100	99	64									
Spartan3E		164	99	64									
Virtex		100	99	64									
Virtex2		100	99	64									
Virtex2p		100	99	64									
VirtexE		100	99	64									
Virtex4		228	99	64									
ProAsicPlus		228											
ProAsic3		229											
ProAsic3E		231											
EC		194	98	64									
ECP		194	98	64									
XP		196	100	64									
MACHXO		196	100	64									

FPGA Peripherals Resource Usage

Port IO 4 x 8 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		54	22	32									
Cyclone2		22	22	32								1	
Stratix		54	22	32									
Stratix2		13	13	32								1	
StratixGX		54	22	32								1	
Spartan2		54	53	32									
Spartan2E		54	53	32									
Spartan3		54	53	32									
Spartan3E		86	53	32									
Virtex		54	53	32									
Virtex2		54	53	32									
Virtex2p		54	53	32									
VirtexE		54	53	32									
Virtex4		118	53	32									
ProAsicPlus		138											
ProAsic3		126											
ProAsic3E		126											
EC		82	53	32									
ECP		82	53	32									
XP		84	54	32									
MACHXO		84	54	32									

Port IO 4 x 32 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		198	70	128								1	
Cyclone2		70	70	128								1	
Stratix		198	70	128									
Stratix2		37	37	128								1	
StratixGX		198	70	128								1	
Spartan2		198	197	128									
Spartan2E		198	197	128									
Spartan3		198	197	128									
Spartan3E		326	197	128									
Virtex		198	197	128									
Virtex2		198	197	128									
Virtex2p		198	197	128									
VirtexE		198	197	128									
Virtex4		70	69										
ProAsicPlus		522											
EC		322	197	128									
ECP		322	197	128									
XP		324	198	128									
MACHXO		324	198	128									

Port IO Tristate 1 x 8 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		19	11	16									
Cyclone2		11	11	16								1	
Stratix		19	11	16								1	
Stratix2		18	18	16								1	
StratixGX		19	11	16								1	
Spartan2		20	19	16									
Spartan2E		20	19	16									
Spartan3		20	19	16									
Spartan3E		36	19	16									
Virtex		20	19	16									
Virtex2		20	19	16									
Virtex2p		20	19	16									
VirtexE		20	19	16									
Virtex4		52	19	16									
ProAsicPlus		52											
ProAsic3		51											
ProAsic3E		51											
EC		34	18	16									
ECP		34	18	16									
XP		36	20	16									
MACHXO		36	20	16									

Port IO Tristate 1 x 32 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		67	35	64									
Cyclone2		35	35	64								1	
Stratix		67	35	64									
Stratix2		35	35	64								1	
StratixGX		67	35	64								1	
Spartan2		68	67	64									
Spartan2E		68	67	64									
Spartan3		68	67	64									
Spartan3E		132	67	64									
Virtex		68	67	64									
Virtex2		68	67	64									
Virtex2p		68	67	64									
VirtexE		68	67	64									
Virtex4		196	67	64									
ProAsicPlus		196											
ProAsic3		197											
ProAsic3E		199											
EC		130	66	64									
ECP		130	66	64									
XP		132	68	64									
MACHXO		132	68	64									

FPGA Peripherals Resource Usage

Port IO Tristate 2 x 8 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		37	21	24									
Cyclone2		21	21	24								1	
Stratix		37	21	24									
Stratix2		20	20	24								1	
StratixGX		38	21	24								1	
Spartan2		36	36	24									
Spartan2E		36	36	24									
Spartan3		36	36	24									
Spartan3E		60	36	24									
Virtex		36	36	24									
Virtex2		36	36	24									
Virtex2p		36	36	24									
VirtexE		36	36	24									
Virtex4		84	36	24									
ProAsicPlus		86											
ProAsic3		85											
ProAsic3E		85											
EC		68	37	24									
ECP		68	37	24									
XP		68	37	24									
MACHXO		68	37	24									

Port IO Tristate 2 x 32 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		133	69	96									
Cyclone2		69	69	96								1	
Stratix		133	69	96									
Stratix2		68	68	96								1	
StratixGX		134	69	96								1	
Spartan2		132	132	96									
Spartan2E		132	132	96									
Spartan3		132	132	96									
Spartan3E		228	132	96									
Virtex		132	132	96									
Virtex2		132	132	96									
Virtex2p		132	132	96									
VirtexE		132	132	96									
Virtex4		36	36										
ProAsicPlus		326											
ProAsic3E		331											
EC		260	133	96									
ECP		260	133	96									
XP		260	133	96									
MACHXO		260	133	96									

Port IO Tristate 4 x 8 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		91	59	64									
Cyclone2		59	59	64								1	
Stratix		91	59	64									
Stratix2		50	50	64								1	
StratixGX		91	59	64								1	
Spartan2		92	90	64									
Spartan2E		92	90	64									
Spartan3		92	90	64									
Spartan3E		156	90	64									
Virtex		92	90	64									
Virtex2		92	90	64									
Virtex2p		92	90	64									
VirtexE		92	90	64									
Virtex4		220	90	64									
ProAsicPlus		240											
ProAsic3		230											
ProAsic3E		230											
EC		148	90	64									
ECP		148	90	64									
XP		148	91	64									
MACHXO		148	91	64									

Port IO Tristate 4 x 32 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		331	203	256									
Cyclone2		204	203	256								1	
Stratix		331	203	256									
Stratix2		171	170	256								1	
StratixGX		331	203	256								1	
Spartan2		332	330	256									
Spartan2E		332	330	256									
Spartan3		332	330	256									
Spartan3E		588	330	256									
Virtex		332	330	256									
Virtex2		332	330	256									
Virtex2p		332	330	256									
VirtexE		332	330	256									
Virtex4		76	74										
ProAsicPlus		912											
EC		580	330	256									
ECP		580	330	256									
XP		580	331	256									
MACHXO		580	331	256									

FPGA Peripherals Resource Usage

Port Output 1x8 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		10	2	8									
Cyclone2		2	2	8								1	
Stratix		10	2	8								1	
Stratix2		9	9	8								1	
StratixGX		10	2	8								1	
Spartan2		10	10	8									
Spartan2E		10	10	8									
Spartan3		10	10	8									
Spartan3E		18	10	8									
Virtex		10	10	8									
Virtex2		10	10	8									
Virtex2p		10	10	8									
VirtexE		10	10	8									
Virtex4		26	10	8									
ProAsicPlus		26											
ProAsic3		26											
ProAsic3E		26											
EC		16	9	8									
ECP		16	9	8									
XP		20	11	8									
MACHXO		20	11	8									

Port Output 1x32 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		34	2	32									
Cyclone2		2	2	32								1	
Stratix		34	2	32									
Stratix2		2	2	32								1	
StratixGX		34	2	32								1	
Spartan2		34	34	32									
Spartan2E		34	34	32									
Spartan3		34	34	32									
Spartan3E		66	34	32									
Virtex		34	34	32									
Virtex2		34	34	32									
Virtex2p		34	34	32									
VirtexE		34	34	32									
Virtex4		98	34	32									
ProAsicPlus		98											
ProAsic3		99											
ProAsic3E		100											
EC		64	33	32									
ECP		64	33	32									
XP		68	35	32									
MACHXO		68	35	32									

Port Output 2x8 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		19	3	16									
Cyclone2		3	3	16								1	
Stratix		19	3	16								1	
Stratix2		3	3	16								1	
StratixGX		19	3	16								1	
Spartan2		20	19	16									
Spartan2E		20	19	16									
Spartan3		20	19	16									
Spartan3E		36	19	16									
Virtex		20	19	16									
Virtex2		20	19	16									
Virtex2p		20	19	16									
VirtexE		20	19	16									
Virtex4		52	19	16									
ProAsicPlus		52											
ProAsic3		51											
ProAsic3E		51											
EC		34	18	16									
ECP		34	18	16									
XP		36	20	16									
MACHXO		36	20	16									

Port Output 2x32 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		67	3	64									
Cyclone2		3	3	64								1	
Stratix		67	3	64									
Stratix2		3	3	64								1	
StratixGX		67	3	64								1	
Spartan2		68	67	64									
Spartan2E		68	67	64									
Spartan3		68	67	64									
Spartan3E		132	67	64									
Virtex		68	67	64									
Virtex2		68	67	64									
Virtex2p		68	67	64									
VirtexE		68	67	64									
Virtex4		196	67	64									
ProAsicPlus		196											
ProAsic3		197											
ProAsic3E		199											
EC		130	66	64									
ECP		130	66	64									
XP		132	68	64									
MACHXO		132	68	64									

Port Output 4x8 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		38	6	32									
Cyclone2		6	6	32								1	
Stratix		38	6	32									
Stratix2		5	5	32								1	
StratixGX		38	6	32								1	
Max3000a	33	33		32									
Max7000b	33	33		32									
Max7000ae	33	33		32									
Max7000s	33	33		32									
Spartan2		38	37	32									
Spartan2E		38	37	32									
Spartan3		38	37	32									
Spartan3E		70	37	32									
Virtex		38	37	32									
Virtex2		38	37	32									
Virtex2p		38	37	32									
VirtexE		38	37	32									
Virtex4		102	37	32									
CoolRunner2	33			32									
CoolRunnerXpla3	33			32									
Xc9500	33			32									
Xc9500XL	33			32									
Xc9500XV	33			32									
ProAsicPlus		104											
ProAsic3		102											
ProAsic3E		102											
EC		66	37	32									
ECP		66	37	32									
XP		68	38	32									
MACHXO		68	38	32									

Port Output 4x32 Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		134	6	128									
Cyclone2		6	6	128								1	
Stratix		134	6	128									
Stratix2		5	5	128								1	
StratixGX		134	6	128								1	
Spartan2		134	133	128									
Spartan2E		134	133	128									
Spartan3		134	133	128									
Spartan3E		262	133	128									
Virtex		134	133	128									
Virtex2		134	133	128									
Virtex2p		134	133	128									
VirtexE		134	133	128									
Virtex4		390	133	128									
ProAsicPlus		392											
ProAsic3		394											
ProAsic3E		398											
EC		258	133	128									
ECP		258	133	128									
XP		260	134	128									
MACHXO		260	134	128									

WB_PWM8

Pulse Width Modulation Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		126	96	69								1	
Cyclone2		97	97	69								1	
Cyclone3		89	89	69									
Stratix		127	97	69								1	
Stratix2		93	93	69								1	
StratixGX		104	100	61								1	
Spartan2		163	129	53									
Spartan2E		163	129	53									
Spartan3		161	126	53									
Spartan3A		161	127	53									
Spartan3E		191	148	69									
Spartan3L		161	127	53									
Virtex		163	129	53									
Virtex2		161	126	53									
Virtex2p		161	126	53									
VirtexE		163	129	53									
Virtex4		161	130	53									
Virtex5		16	16	16									
ProAsicPlus		372											
ProAsic3		341											
ProAsic3E		342											
EC		150	142	69									
ECP		150	142	69									
ECP2		138	93	69									
ECP2M		138	93	69									
MACHXO		156	143										
XP		136	121	69									
SC		152	135	61									

WB_PWMX

Extended Pulse Width Modulation Controller Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		143	143	73								1	
Cyclone2		151	151	73								1	
Cyclone3		135	135	73									
Stratix		156	153	73								1	
Stratix2		133	133	73								1	
StratixGX		150	149	73								1	
Spartan2		221	180	65									
Spartan2E		221	180	65									
Spartan3		223	178	65									
Spartan3A		219	178	65									
Spartan3E		237	189	73									
Spartan3L		219	183	65									
Virtex		221	180	65									
Virtex2		223	182	65									
Virtex2p		223	182	65									
VirtexE		221	180	65									
Virtex4		225	181	65									
Virtex5		8	8	8									
ProAsicPlus		471											
ProAsic3		454											
ProAsic3E		456											
EC		198	183	73									
ECP		198	183	73									
ECP2		190	148	73									
ECP2M		190	148	73									
MACHXO		200	186										
XP		178	161	73									
SC		208	181	73									

WB_UART8

UART Buffered with handshake, Wishbone

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		564	444	385								8	
Cyclone2		325	314	243		2						12	
Cyclone3		467	467	433									
Stratix		565	444	385								12	
Stratix2		356	347	385								12	
StratixGX		565	444	385								12	
Spartan2		571	440	173									
Spartan2E		571	440	173									
Spartan3		581	443	173									
Spartan3A		701	560	221									
Spartan3E		623	474	193									
Spartan3L		699	558	221									
Virtex		571	440	173									
Virtex2		581	443	173									
Virtex2p		579	443	173									
VirtexE		571	440	173									
Virtex4		581	443	173									
Virtex5		20	20	20									
ProAsicPlus		1652											
ProAsic3		1291											
ProAsic3E		1304											
EC		434	342	198									
ECP		434	342	198									
ECP2		542	401	241									
ECP2M		542	401	241									
MACHXO		438	331										
XP		470	333	193									
SC		410	316	193									

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
19-May-2005	1.02	Renamed EMAC variants to EMAC8 and regenerated resource usage information
6-Jun-2005	1.03	EMAC32, WB_PWMX and WB_UART8 added Added MAX2 resource usage
15-Sep-2005	1.04	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage Regenerated resource usage statistics to reflect the changes to SPI_W
20-Dec-2005	1.05	Added ProAsic3
28-Mar-2006	1.06	Added ProAsic3E, Statistic. VGA32_16BPP, I2S_W, BT656 VGA32_TFT, WB_MULTIMASTER components added.
20-Apr-2006	1.07	Tools Utilized section added
16-Jun-2006	1.08	Proasic3E and XP added
1-Aug-2006	1.09	MACHXO added
23-Aug-2007	1.10	WB_IRCODER added, Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.11	Altium Designer Summer 08 SP1