



FPGA Logic Primitive Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Logic Primitive cores.

Core Reference
CR0136 (v1.11) December 19, 2008

Logic Primitive

The available Logic Primitive cores are listed as follows:

- [AND Gates](#)
- [Inverters](#)
- [NAND Gates](#)
- [NOR Gates](#)
- [OR Gates](#)
- [Sum of Product](#)
- [True/Complement](#)
- [XNOR Gates](#)
- [XOR Gates](#)

AND Gates

The available AND Gates cores are listed as follows:

AND2B	AND2DB	AND2DS	AND2N1B
AND2N1S	AND2N2B	AND2N2S	AND2S
AND3B	AND3DB	AND3DS	AND3N1B
AND3N1S	AND3N2B	AND3N2S	AND3N3B
AND3N3S	AND3S	AND4B	AND4DB
AND4DS	AND4N1B	AND4N1S	AND4N2B
AND4N2S	AND4N3B	AND4N3S	AND4N4B
AND4N4S	AND4S	AND5B	AND5N1B
AND5N1S	AND5N2B	AND5N2S	AND5N3B
AND5N3S	AND5N4B	AND5N4S	AND5N5B
AND5N5S	AND5S	AND6B	AND6S
AND7B	AND7S	AND8B	AND8S
AND9B	AND9S	AND12B	AND12S
AND16B	AND16S	AND32B	

FPGA Logic Primitive Resource Usage

Inverters

The available Inverters cores are listed as follows:

INV	INV2B	INV2S	INV3B
INV3S	INV4B	INV4S	INV5B
INV5S	INV6B	INV6S	INV7B
INV7S	INV8B	INV8S	INV9B
INV9S	INV10B	INV10S	INV12B
INV12S	INV16B	INV16S	INV32B

NAND Gates

The available NAND Gates cores are listed as follows:

NAND2B	NAND2N1B	NAND2N1S	NAND2N2B
NAND2N2S	NAND2S	NAND3B	NAND3N1B
NAND3N1S	NAND3N2B	NAND3N2S	NAND3N3B
NAND3N3S	NAND3S	NAND4B	NAND4N1B
NAND4N1S	NAND4N2B	NAND4N2S	NAND4N3B
NAND4N3S	NAND4N4B	NAND4N4S	NAND4S
NAND5B	NAND5N1B	NAND5N1S	NAND5N2B
NAND5N2S	NAND5N3B	NAND5N3S	NAND5N4B
NAND5N4S	NAND5N5B	NAND5N5S	NAND5S
NAND6B	NAND6S	NAND7B	NAND7S
NAND8B	NAND8S	NAND9B	NAND9S
NAND12B	NAND12S	NAND16B	NAND16S
NAND32B			

NOR Gates

The available NOR Gates cores are listed as follows:

NOR2B	NOR2N1B	NOR2N1S	NOR2N2B
NOR2N2S	NOR2S	NOR3B	NOR3N1B
NOR3N1S	NOR3N2B	NOR3N2S	NOR3N3B
NOR3N3S	NOR3S	NOR4B	NOR4N1B
NOR4N1S	NOR4N2B	NOR4N2S	NOR4N3B
NOR4N3S	NOR4N4B	NOR4N4S	NOR4S
NOR5B	NOR5N1B	NOR5N1S	NOR5N2B
NOR5N2S	NOR5N3B	NOR5N3S	NOR5N4B

NOR5N4S	NOR5N5B	NOR5N5S	NOR5S
NOR6B	NOR6S	NOR7B	NOR7S
NOR8B	NOR8S	NOR9B	NOR9S
NOR12B	NOR12S	NOR16B	NOR16S
NOR32B			

OR Gates

The available OR Gates cores are listed as follows:

OR2B	OR2DB	OR2DS	OR2N1B
OR2N1S	OR2N2B	OR2N2S	OR2S
OR3B	OR3DB	OR3DS	OR3N1B
OR3N1S	OR3N2B	OR3N2S	OR3N3B
OR3N3S	OR3S	OR4B	OR4DB
OR4DS	OR4N1B	OR4N1S	OR4N2B
OR4N2S	OR4N3B	OR4N3S	OR4N4B
OR4N4S	OR4S	OR5B	OR5N1B
OR5N1S	OR5N2B	OR5N2S	OR5N3B
OR5N3S	OR5N4B	OR5N4S	OR5N5B
OR5N5S	OR5S	OR6B	OR6S
OR7B	OR7S	OR8B	OR8S
OR9B	OR9S	OR12B	OR12S
OR16B	OR16S	OR32B	

Sum of Product

The available Sum of Product cores are listed as follows:

SOP2_2B	SOP2_2S	SOP2_3B	SOP2_3S
SOP2_4B	SOP2_4S	SOP4_2B	SOP4_2S

True/Complement

The available True/Complement cores are listed as follows:

[TCZO](#)

XNOR Gates

The available XNOR Gates cores are listed as follows:

XNOR2B	XNOR2N1B	XNOR2N1S	XNOR2N2B
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XNOR2N2S	XNOR2S	XNOR3B	XNOR3N1B
XNOR3N1S	XNOR3N2B	XNOR3N2S	XNOR3N3B
XNOR3N3S	XNOR3S	XNOR4B	XNOR4N1B
XNOR4N1S	XNOR4N2B	XNOR4N2S	XNOR4N3B
XNOR4N3S	XNOR4N4B	XNOR4N4S	XNOR4S
XNOR5B	XNOR5N1B	XNOR5N1S	XNOR5N2B
XNOR5N2S	XNOR5N3B	XNOR5N3S	XNOR5N4B
XNOR5N4S	XNOR5N5B	XNOR5N5S	XNOR5S
XNOR6B	XNOR6S	XNOR7B	XNOR7S
XNOR8B	XNOR8S	XNOR9B	XNOR9S
XNOR12B	XNOR12S	XNOR16B	XNOR16S
XNOR32B			

XOR Gates

The available XOR Gates cores are listed as follows:

XOR2B	XOR2N1B	XOR2N1S	XOR2N2B
XOR2N2S	XOR2S	XOR3B	XOR3N1B
XOR3N1S	XOR3N2B	XOR3N2S	XOR3N3B
XOR3N3S	XOR3S	XOR4B	XOR4N1B
XOR4N1S	XOR4N2B	XOR4N2S	XOR4N3B
XOR4N3S	XOR4N4B	XOR4N4S	XOR4S
XOR5B	XOR5N1B	XOR5N1S	XOR5N2B
XOR5N2S	XOR5N3B	XOR5N3S	XOR5N4B
XOR5N4S	XOR5N5B	XOR5N5S	XOR5S
XOR6B	XOR6S	XOR7B	XOR7S
XOR8B	XOR8S	XOR9B	XOR9S
XOR12B	XOR12S	XOR16B	XOR16S
XOR32B			

AND2B

2-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L													
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3													
ProAsic3E													
Fusion													
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND2DB

2-Input AND/NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L													
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4											
ECP		4											
ECP2		4	2										
ECP2M		4	2										
SC		4	2										
MACHXO		4	2										
XP		4	2										
XP2		4	2										

AND2DS

2-Input AND/NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L													
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4											
ECP		4											
ECP2		4	2										
ECP2M		4	2										
SC		4	2										
MACHXO		4	2										
XP		4	2										
XP2		4	2										

FPGA Logic Primitive Resource Usage

AND2N1B

2-Input AND Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L													
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND2N1S

2-Input AND Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L													
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND2N2B

2-Input AND Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND2N2S

2-Input AND Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND2S

2-Input AND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND3B

3-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3													
ProAsic3E													
Fusion													
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND3DB

3-Input AND/NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

AND3DS

3-Input AND/NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

AND3N1B

3-Input AND Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND3N1S

3-Input AND Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND3N2B

3-Input AND Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND3N2S

3-Input AND Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND3N3B

3-Input AND Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND3N3S

3-Input AND Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND3S

3-Input AND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND4B

4-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND4DB

4-Input AND/NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2											
ECP		2											
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

AND4DS

4-Input AND/NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2											
ECP		2											
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

AND4N1B

4-Input AND Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND4N1S

4-Input AND Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND4N2B

4-Input AND Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND4N2S

4-Input AND Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND4N3B

4-Input AND Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND4N3S

4-Input AND Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND4N4B

4-Input AND Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND4N4S

4-Input AND Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

AND4S

4-Input AND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

AND5B

5-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

AND5N1B

5-Input AND Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

AND5N1S

5-Input AND Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

AND5N2B

5-Input AND Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

AND5N2S

5-Input AND Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

AND5N3B

5-Input AND Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

AND5N3S

5-Input AND Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

AND5N4B

5-Input AND Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

AND5N4S

5-Input AND Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

AND5N5B

5-Input AND Gate with Active Low A, B, C, D and E Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

AND5N5S

5-Input AND Gate with Active Low A, B, C, D and E Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

AND5S

5-Input AND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

AND6B

6-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

AND6S

6-Input AND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

AND7B

7-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			3										
ProAsic3			3										
ProAsic3E			3										
Fusion			3										
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

AND7S

7-Input AND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			3										
ProAsic3			3										
ProAsic3E			3										
Fusion			3										
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

AND8B

8-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

AND8S

8-Input AND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

AND9B

9-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

AND9S

9-Input AND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

AND12B

12-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4											
ECP		4											
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

FPGA Logic Primitive Resource Usage

AND12S

12-Input AND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4											
ECP		4											
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

AND16B

16-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			8										
ProAsic3			8										
ProAsic3E			8										
Fusion			8										
EC			6										
ECP			6										
ECP2			6	5									
ECP2M			6	5									
SC			6	5									
MACHXO			6	5									
XP			6	5									
XP2			6	5									

FPGA Logic Primitive Resource Usage

AND16S

16-Input AND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			8										
ProAsic3			8										
ProAsic3E			8										
Fusion			8										
EC			6										
ECP			6										
ECP2			6	5									
ECP2M			6	5									
SC			6	5									
MACHXO			6	5									
XP			6	5									
XP2			6	5									

AND32B

32-Input AND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9										
Cyclone		11	11										
Cyclone2		11	11										
Cyclone3		11	11										
Stratix		11	11										
Stratix2		10	10										
Stratix3			9										
StratixGX		11	11										
Stratix2GX			7										
Max2		11	11										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		12	11										
Spartan2E		12	11										
Spartan3		12	11										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		12	11										
Virtex2		12	11										
Virtex2p		12	11										
VirtexE		12	11										
Virtex4		12	11										
Virtex5			8										
CoolRunner2	2												
CoolRunnerXpla3	31												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		12											
ECP		12											
ECP2		14	12										
ECP2M		14	12										
SC		12	11										
MACHXO		12	11										
XP		12	11										
XP2		12	11										

FPGA Logic Primitive Resource Usage

INV

Inverter

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		1										
Cyclone		1	1									
Cyclone2		1	1									
Cyclone3		1	1									
Stratix		1	1									
Stratix2		1	1									
Stratix3		1										
StratixGX		1	1									
Stratix2gx		1										
Max2		1										
Max3000a	1	1										
Max7000b	1	1										
Max7000ae	1	1										
Max7000s	1	1										
Spartan2		1	1									
Spartan2E		1	1									
Spartan3		1	1									
Spartan3A		1										
Spartan3adsp		1										
Spartan3an		1										
Spartan3E		1	1									
Spartan3L		1	1									
Virtex		1	1									
Virtex2		1	1									
Virtex2p		1	1									
VirtexE		1	1									
Virtex4		1	1									
Virtex5		1	1									
CoolRunner2	1	1										
CoolRunnerXpla3	1	1										
Xc9500	1	1										
Xc9500XL	1	1										
Xc9500XV	1	1										
ProAsicPlus		1	1									
ProAsic3		1	1									
ProAsic3E		1										
Fusion		1										
EC		1	1									
ECP		1	1									
ECP2		1	1									
ECP2M		1	1									
Sc		1										
MACHXO		1	1									
XP		1	1									
Xp2		1										

INV2B

2-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		2	2										
Spartan3L													
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5													
CoolRunner2	2	2											
CoolRunnerXpla3	2	2											
Xc9500	2	2											
Xc9500XL	2	2											
Xc9500XV	2	2											
ProAsicPlus		2	2										
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		4	2										
ECP2M		4	2										
SC		4	2										
MACHXO		4	2										
XP		4	2										
XP2		4	2										

FPGA Logic Primitive Resource Usage

INV2S

2-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		2	2										
Spartan3L													
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5													
CoolRunner2	2	2											
CoolRunnerXpla3	2	2											
Xc9500	2	2											
Xc9500XL	2	2											
Xc9500XV	2	2											
ProAsicPlus		2	2										
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		4	2										
ECP2M		4	2										
SC		4	2										
MACHXO		4	2										
XP		4	2										
XP2		4	2										

INV3B

3-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			3										
StratixGX		3	3										
Stratix2GX			3										
Max2		3	3										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		3	3										
Spartan3L													
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5													
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		6	3										
ECP2M		6	3										
SC		6	3										
MACHXO		6	3										
XP		6	3										
XP2		6	3										

FPGA Logic Primitive Resource Usage

INV3S

3-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			3										
StratixGX		3	3										
Stratix2GX			3										
Max2		3	3										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		3	3										
Spartan3L													
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5													
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		6	3										
ECP2M		6	3										
SC		6	3										
MACHXO		6	3										
XP		6	3										
XP2		6	3										

INV4B

4-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			4										
StratixGX		4	4										
Stratix2GX			4										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		4	4										
Spartan3L													
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5													
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		8	4										
ECP2M		8	4										
SC		8	4										
MACHXO		8	4										
XP		8	4										
XP2		8	4										

FPGA Logic Primitive Resource Usage

INV4S

4-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			4										
StratixGX		4	4										
Stratix2GX			4										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		4	4										
Spartan3L													
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5													
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		8	4										
ECP2M		8	4										
SC		8	4										
MACHXO		8	4										
XP		8	4										
XP2		8	4										

INV5B

5-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			5										
StratixGX		5	5										
Stratix2GX			5										
Max2		5	5										
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		5	5										
Spartan3L													
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5													
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		10	5										
ECP2M		10	5										
SC		10	5										
MACHXO		10	5										
XP		10	5										
XP2		10	5										

FPGA Logic Primitive Resource Usage

INV5S

5-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			5										
StratixGX		5	5										
Stratix2GX			5										
Max2		5	5										
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		5	5										
Spartan3L													
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5													
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		10	5										
ECP2M		10	5										
SC		10	5										
MACHXO		10	5										
XP		10	5										
XP2		10	5										

INV6B

6-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6										
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3			6										
StratixGX		6	6										
Stratix2GX			6										
Max2		6	6										
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		6	6										
Spartan3L													
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5													
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		12	6										
ECP2M		12	6										
SC		12	6										
MACHXO		12	6										
XP		12	6										
XP2		12	6										

FPGA Logic Primitive Resource Usage

INV6S

6-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6										
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3			6										
StratixGX		6	6										
Stratix2GX			6										
Max2		6	6										
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		6	6										
Spartan3L													
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5													
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		12	6										
ECP2M		12	6										
SC		12	6										
MACHXO		12	6										
XP		12	6										
XP2		12	6										

INV7B

7-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7										
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3			7										
StratixGX		7	7										
Stratix2GX			7										
Max2		7	7										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		7	7										
Spartan3L													
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5													
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7											
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		14	7										
ECP2M		14	7										
SC		14	7										
MACHXO		14	7										
XP		14	7										
XP2		14	7										

FPGA Logic Primitive Resource Usage

INV7S

7-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7										
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3			7										
StratixGX		7	7										
Stratix2GX			7										
Max2		7	7										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		7	7										
Spartan3L													
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5													
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7											
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		14	7										
ECP2M		14	7										
SC		14	7										
MACHXO		14	7										
XP		14	7										
XP2		14	7										

INV8B

8-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8										
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3			8										
StratixGX		8	8										
Stratix2GX			8										
Max2		8	8										
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		8	8										
Spartan3L													
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5													
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		16	8										
ECP2M		16	8										
SC		16	8										
MACHXO		16	8										
XP		16	8										
XP2		16	8										

FPGA Logic Primitive Resource Usage

INV8S

8-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8										
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3			8										
StratixGX		8	8										
Stratix2GX			8										
Max2		8	8										
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		8	8										
Spartan3L													
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5													
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		16	8										
ECP2M		16	8										
SC		16	8										
MACHXO		16	8										
XP		16	8										
XP2		16	8										

INV9B

9-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9										
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3			9										
StratixGX		9	9										
Stratix2GX			9										
Max2		9	9										
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		9	9										
Spartan3L													
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5													
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		18	9										
ECP2M		18	9										
SC		18	9										
MACHXO		18	9										
XP		18	9										
XP2		18	9										

FPGA Logic Primitive Resource Usage

INV9S

9-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9										
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3			9										
StratixGX		9	9										
Stratix2GX			9										
Max2		9	9										
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		9	9										
Spartan3L													
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5													
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		18	9										
ECP2M		18	9										
SC		18	9										
MACHXO		18	9										
XP		18	9										
XP2		18	9										

INV10B

10-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10										
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3			10										
StratixGX		10	10										
Stratix2GX			10										
Max2		10	10										
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		10	10										
Spartan3L													
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5													
CoolRunner2	10	10											
CoolRunnerXpla3	10	10											
Xc9500	10	10											
Xc9500XL	10	10											
Xc9500XV	10	10											
ProAsicPlus		10	10										
ProAsic3		10											
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		20	10										
ECP2M		20	10										
SC		20	10										
MACHXO		20	10										
XP		20	10										
XP2		20	10										

FPGA Logic Primitive Resource Usage

INV10S

10-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10										
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3			10										
StratixGX		10	10										
Stratix2GX			10										
Max2		10	10										
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		10	10										
Spartan3L													
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5													
CoolRunner2	10	10											
CoolRunnerXpla3	10	10											
Xc9500	10	10											
Xc9500XL	10	10											
Xc9500XV	10	10											
ProAsicPlus		10	10										
ProAsic3		10											
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		20	10										
ECP2M		20	10										
SC		20	10										
MACHXO		20	10										
XP		20	10										
XP2		20	10										

INV12B

12-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			12										
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3			12										
StratixGX		12	12										
Stratix2GX			12										
Max2		12	12										
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		12	12										
Spartan3L													
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5													
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		24	12										
ECP2M		24	12										
SC		24	12										
MACHXO		24	12										
XP		24	12										
XP2		24	12										

FPGA Logic Primitive Resource Usage

INV12S

12-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			12										
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3			12										
StratixGX		12	12										
Stratix2GX			12										
Max2		12	12										
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		12	12										
Spartan3L													
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5													
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		24	12										
ECP2M		24	12										
SC		24	12										
MACHXO		24	12										
XP		24	12										
XP2		24	12										

INV16B

16-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16										
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3			16										
StratixGX		16	16										
Stratix2GX			16										
Max2		16	16										
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		16	16										
Spartan3L													
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5													
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		32	16										
ECP2M		32	16										
SC		32	16										
MACHXO		32	16										
XP		32	16										
XP2		32	16										

FPGA Logic Primitive Resource Usage

INV16S

16-Bit Inverter, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16										
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3			16										
StratixGX		16	16										
Stratix2GX			16										
Max2		16	16										
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		16	16										
Spartan3L													
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5													
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		32	16										
ECP2M		32	16										
SC		32	16										
MACHXO		32	16										
XP		32	16										
XP2		32	16										

INV32B

32-Bit Inverter, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32										
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3			32										
StratixGX		32	32										
Stratix2GX			32										
Max2		32	32										
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A													
Spartan3ADSP													
Spartan3AN													
Spartan3E		32	32										
Spartan3L													
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5													
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32											
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		64	32										
ECP2M		64	32										
SC		64	32										
MACHXO		64	32										
XP		64	32										
XP2		64	32										

FPGA Logic Primitive Resource Usage

NAND2B

2-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3													
ProAsic3E													
Fusion													
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND2N1B

2-Input NAND Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND2N1S

2-Input NAND Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5													
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND2N2B

2-Input NAND Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5													
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND2N2S

2-Input NAND Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND2S

2-Input NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND3B

3-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3													
ProAsic3E													
Fusion													
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND3N1B

3-Input NAND Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND3N1S

3-Input NAND Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND3N2B

3-Input NAND Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND3N2S

3-Input NAND Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND3N3B

3-Input NAND Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND3N3S

3-Input NAND Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND3S

3-Input NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND4B

4-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND4N1B

4-Input NAND Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND4N1S

4-Input NAND Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND4N2B

4-Input NAND Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND4N2S

4-Input NAND Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND4N3B

4-Input NAND Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND4N3S

4-Input NAND Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND4N4B

4-Input NAND Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND4N4S

4-Input NAND Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NAND4S

4-Input NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NAND5B

5-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NAND5N1B

5-Input NAND Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NAND5N1S

5-Input NAND Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NAND5N2B

5-Input NAND Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NAND5N2S

5-Input NAND Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NAND5N3B

5-Input NAND Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NAND5N3S

5-Input NAND Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NAND5N4B

5-Input NAND Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NAND5N4S

5-Input NAND Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NAND5N5B

5-Input NAND Gate with Active Low A, B, C, D and E Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NAND5N5S

5-Input NAND Gate with Active Low A, B, C, D and E Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NAND5S

5-Input NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NAND6B

6-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NAND6S

6-Input NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NAND7B

7-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			3										
ProAsic3			3										
ProAsic3E			3										
Fusion			3										
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NAND7S

7-Input NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			3										
ProAsic3			3										
ProAsic3E			3										
Fusion			3										
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NAND8B

8-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

NAND8S

8-Input NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

NAND9B

9-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

NAND9S

9-Input NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

NAND12B

12-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

NAND12S

12-Input NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

FPGA Logic Primitive Resource Usage

NAND16B

16-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			8										
ProAsic3			8										
ProAsic3E			8										
Fusion			8										
EC		6	5										
ECP		6	5										
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

NAND16S

16-Input NAND Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			8										
ProAsic3			8										
ProAsic3E			8										
Fusion			8										
EC		6	5										
ECP		6	5										
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

FPGA Logic Primitive Resource Usage

NAND32B

32-Input NAND Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9										
Cyclone		11	11										
Cyclone2		11	11										
Cyclone3		11	11										
Stratix		11	11										
Stratix2		10	10										
Stratix3			9										
StratixGX		11	11										
Stratix2GX			7										
Max2		11	11										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		12	11										
Spartan2E		12	11										
Spartan3		12	11										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		12	11										
Virtex2		12	11										
Virtex2p		12	11										
VirtexE		12	11										
Virtex4		12	11										
Virtex5			8										
CoolRunner2	2												
CoolRunnerXpla3	31												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		12	11										
ECP		12	11										
ECP2		14	12										
ECP2M		14	12										
SC		12	11										
MACHXO		12	11										
XP		12	11										
XP2		12	11										

NOR2B

2-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3													
ProAsic3E													
Fusion													
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR2N1B

2-Input NOR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR2N1S

2-Input NOR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR2N2B

2-Input NOR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR2N2S

2-Input NOR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR2S

2-Input NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR3B

3-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3													
ProAsic3E													
Fusion													
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR3N1B

3-Input NOR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR3N1S

3-Input NOR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR3N2B

3-Input NOR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR3N2S

3-Input NOR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR3N3B

3-Input NOR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR3N3S

3-Input NOR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR3S

3-Input NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR4B

4-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR4N1B

4-Input NOR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR4N1S

4-Input NOR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR4N2B

4-Input NOR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR4N2S

4-Input NOR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR4N3B

4-Input NOR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR4N3S

4-Input NOR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR4N4B

4-Input NOR Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR4N4S

4-Input NOR Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

NOR4S

4-Input NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

NOR5B

5-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NOR5N1B

5-Input NOR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NOR5N1S

5-Input NOR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NOR5N2B

5-Input NOR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NOR5N2S

5-Input NOR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NOR5N3B

5-Input NOR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NOR5N3S

5-Input NOR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NOR5N4B

5-Input NOR Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NOR5N4S

5-Input NOR Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NOR5N5B

5-Input NOR Gate with Active Low A, B, C, D and E Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NOR5N5S

5-Input NOR Gate with Active Low A, B, C, D and E Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NOR5S

5-Input NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NOR6B

6-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NOR6S

6-Input NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NOR7B

7-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			3										
ProAsic3			3										
ProAsic3E			3										
Fusion			3										
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

NOR7S

7-Input NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			3										
ProAsic3			3										
ProAsic3E			3										
Fusion			3										
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

NOR8B

8-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

NOR8S

8-Input NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

NOR9B

9-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

NOR9S

9-Input NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

NOR12B

12-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

FPGA Logic Primitive Resource Usage

NOR12S

12-Input NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

NOR16B

16-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			8										
ProAsic3			8										
ProAsic3E			8										
Fusion			8										
EC		6	5										
ECP		6	5										
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

FPGA Logic Primitive Resource Usage

NOR16S

12-Input NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			8										
ProAsic3			8										
ProAsic3E			8										
Fusion			8										
EC		6	5										
ECP		6	5										
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

NOR32B

32-Input NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9										
Cyclone		11	11										
Cyclone2		11	11										
Cyclone3		11	11										
Stratix		11	11										
Stratix2		10	10										
Stratix3			9										
StratixGX		11	11										
Stratix2GX			7										
Max2		11	11										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		12	11										
Spartan2E		12	11										
Spartan3		12	11										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		12	11										
Virtex2		12	11										
Virtex2p		12	11										
VirtexE		12	11										
Virtex4		12	11										
Virtex5			8										
CoolRunner2	2												
CoolRunnerXpla3	31												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		12	11										
ECP		12	11										
ECP2		14	12										
ECP2M		14	12										
SC		12	11										
MACHXO		12	11										
XP		12	11										
XP2		12	11										

FPGA Logic Primitive Resource Usage

OR2B

2-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3													
ProAsic3E													
Fusion													
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR2DB

2-Input OR/NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4	2										
ECP		4	2										
ECP2		4	2										
ECP2M		4	2										
SC		4	2										
MACHXO		4	2										
XP		4	2										
XP2		4	2										

FPGA Logic Primitive Resource Usage

OR2DS

2-Input OR/NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4	2										
ECP		4	2										
ECP2		4	2										
ECP2M		4	2										
SC		4	2										
MACHXO		4	2										
XP		4	2										
XP2		4	2										

OR2N1B

2-Input OR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR2N1S

2-Input OR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR2N2B

2-Input OR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR2N2S

2-Input OR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR2S

2-Input OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR3B

3-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3													
ProAsic3E													
Fusion													
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR3DB

3-Input OR/NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

OR3DS

3-Input OR/NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

OR3N1B

3-Input OR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR3N1S

3-Input OR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR3N2B

3-Input OR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR3N2S

3-Input OR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR3N3B

3-Input OR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR3N3S

3-Input OR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR3S

3-Input OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A													
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR4B

4-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR4DB

4-Input OR/NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

OR4DS

4-Input OR/NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

OR4N1B

4-Input OR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR4N1S

4-Input OR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR4N2B

4-Input OR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR4N2S

4-Input OR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR4N3B

4-Input OR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR4N3S

4-Input OR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR4N4B

4-Input OR Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR4N4S

4-Input OR Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

OR4S

4-Input OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

OR5B

5-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

OR5N1B

5-Input OR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

OR5N1S

5-Input OR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

OR5N2B

5-Input OR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

OR5N2S

5-Input OR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

OR5N3B

5-Input OR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

OR5N3S

5-Input OR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

OR5N4B

5-Input OR Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

OR5N4S

5-Input OR Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

OR5N5B

5-Input OR Gate with Active Low A, B, C, D and E Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

OR5N5S

5-Input OR Gate with Active Low A, B, C, D and E Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

OR5S

5-Input OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

OR6B

6-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

OR6S

6-Input OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

OR7B

7-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			3										
ProAsic3			3										
ProAsic3E			3										
Fusion			3										
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

OR7S

7-Input OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			3										
ProAsic3			3										
ProAsic3E			3										
Fusion			3										
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

OR8B

8-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

OR8S

8-Input OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

OR9B

9-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

OR9S

9-Input OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

OR12B

12-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

OR12S

12-Input OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

FPGA Logic Primitive Resource Usage

OR16B

16-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			8										
ProAsic3			8										
ProAsic3E			8										
Fusion			8										
EC		6	5										
ECP		6	5										
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

OR16S

16-Input OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			8										
ProAsic3			8										
ProAsic3E			8										
Fusion			8										
EC		6	5										
ECP		6	5										
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

FPGA Logic Primitive Resource Usage

OR32B

32-Input OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9										
Cyclone		11	11										
Cyclone2		11	11										
Cyclone3		11	11										
Stratix		11	11										
Stratix2		10	10										
Stratix3			9										
StratixGX		11	11										
Stratix2GX			7										
Max2		11	11										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		12	11										
Spartan2E		12	11										
Spartan3		12	11										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		12	11										
Virtex2		12	11										
Virtex2p		12	11										
VirtexE		12	11										
Virtex4		12	11										
Virtex5			8										
CoolRunner2	2												
CoolRunnerXpla3	31												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		12	11										
ECP		12	11										
ECP2		14	12										
ECP2M		14	12										
SC		12	11										
MACHXO		12	11										
XP		12	11										
XP2		12	11										

SOP2_2B

Sum of Product, two 2-inputs AND-OR-INVERT Gates Combination, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

SOP2_2S

Sum of Product, two 2-inputs AND-OR-INVERT Gates Combination, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

SOP2_3B

Sum of Product, two 3-inputs AND-OR-INVERT Gates Combination, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

SOP2_3S

Sum of Product, two 3-inputs AND-OR-INVERT Gates Combination, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

SOP2_4B

Sum of Product, two 4-Inputs AND-OR-INVERT Gates Combination, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

SOP2_4S

Sum of Product, two 4-Inputs AND-OR-INVERT Gates Combination, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

SOP4_2B

Sum of Product, four 2-inputs AND-OR-INVERT Gates Combination, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

SOP4_2S

Sum of Product, four 2-inputs AND-OR-INVERT Gates Combination, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

TCZO

True/Complement, Zero/One Element

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR2B

2-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR2N1B

2-Input Exclusive-NOR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR2N1S

2-Input Exclusive-NOR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR2N2B

2-Input Exclusive-NOR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR2N2S

2-Input Exclusive-NOR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR2S

2-Input Exclusive-NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR3B

3-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR3N1B

3-Input Exclusive-NOR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR3N1S

3-Input Exclusive-NOR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR3N2B

3-Input Exclusive-NOR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR3N2S

3-Input Exclusive-NOR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR3N3B

3-Input Exclusive-NOR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR3N3S

3-Input Exclusive-NOR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR3S

3-Input Exclusive-NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR4B

4-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR4N1B

4-Input Exclusive-NOR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR4N1S

4-Input Exclusive-NOR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR4N2B

4-Input Exclusive-NOR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR4N2S

4-Input Exclusive-NOR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR4N3B

4-Input Exclusive-NOR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR4N3S

4-Input Exclusive-NOR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR4N4B

4-Input Exclusive-NOR Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR4N4S

4-Input Exclusive-NOR Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			3										
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XNOR4S

4-Input Exclusive-NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XNOR5B

5-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XNOR5N1B

5-Input Exclusive-NOR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XNOR5N1S

5-Input Exclusive-NOR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XNOR5N2B

5-Input Exclusive-NOR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XNOR5N2S

5-Input Exclusive-NOR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XNOR5N3B

5-Input Exclusive-NOR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XNOR5N3S

5-Input Exclusive-NOR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XNOR5N4B

5-Input Exclusive-NOR Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XNOR5N4S

5-Input Exclusive-NOR Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XNOR5N5B

5-Input Exclusive-NOR Gate with Active Low A, B, C, D and E Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XNOR5N5S

5-Input Exclusive-NOR Gate with Active Low A, B, C, D and E Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XNOR5S

5-Input Exclusive-NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XNOR6B

6-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		5											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XNOR6S

6-Input Exclusive-NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		5											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XNOR7B

7-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		6											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XNOR7S

7-Input Exclusive-NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		6											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XNOR8B

8-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		7											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

XNOR8S

8-Input Exclusive-NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		7											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

XNOR9B

9-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		8											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

XNOR9S

9-Input Exclusive-NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		8											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

XNOR12B

12-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	3												
CoolRunnerXpla3	3												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		11											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

XNOR12S

12-Input Exclusive-NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	3												
CoolRunnerXpla3	3												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		11											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

FPGA Logic Primitive Resource Usage

XNOR16B

16-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	5												
CoolRunnerXpla3	5												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		15											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		6	5										
ECP		6	5										
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

XNOR16S

16-Input Exclusive-NOR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	5												
CoolRunnerXpla3	5												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		15											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		6	5										
ECP		6	5										
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

FPGA Logic Primitive Resource Usage

XNOR32B

32-Input Exclusive-NOR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9										
Cyclone		11	11										
Cyclone2		11	11										
Cyclone3		11	11										
Stratix		11	11										
Stratix2		10	10										
Stratix3			9										
StratixGX		11	11										
Stratix2GX			7										
Max2		11	11										
Max3000a	11	11											
Max7000b	11	11											
Max7000ae	11	11											
Max7000s	11	11											
Spartan2		12	11										
Spartan2E		12	11										
Spartan3		12	11										
Spartan3A		12	11										
Spartan3ADSP		12	11										
Spartan3AN		12	11										
Spartan3E		18	11										
Spartan3L		12	11										
Virtex		12	11										
Virtex2		12	11										
Virtex2p		12	11										
VirtexE		12	11										
Virtex4		12	11										
Virtex5			8										
CoolRunner2	12												
CoolRunnerXpla3	12												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		31											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		12	11										
ECP		12	11										
ECP2		12	11										
ECP2M		12	11										
SC		12	11										
MACHXO		12	11										
XP		12	11										
XP2		12	11										

XOR2B

2-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR2N1B

2-Input Exclusive-OR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR2N1S

2-Input Exclusive-OR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR2N2B

2-Input Exclusive-OR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR2N2S

2-Input Exclusive-OR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR2S

2-Input Exclusive-OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR3B

3-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR3N1B

3-Input Exclusive-OR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR3N1S

3-Input Exclusive-OR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR3N2B

3-Input Exclusive-OR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR3N2S

3-Input Exclusive-OR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR3N3B

3-Input Exclusive-OR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR3N3S

3-Input Exclusive-OR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR3S

3-Input Exclusive-OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR4B

4-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR4N1B

4-Input Exclusive-OR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR4N1S

4-Input Exclusive-OR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR4N2B

4-Input Exclusive-OR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR4N2S

4-Input Exclusive-OR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR4N3B

4-Input Exclusive-OR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR4N3S

4-Input Exclusive-OR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR4N4B

4-Input Exclusive-OR Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR4N4S

4-Input Exclusive-OR Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus			3										
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

FPGA Logic Primitive Resource Usage

XOR4S

4-Input Exclusive-OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2	1										
Spartan2E		2	1										
Spartan3		2	1										
Spartan3A		2	1										
Spartan3ADSP		2	1										
Spartan3AN		2	1										
Spartan3E		2	1										
Spartan3L		2	1										
Virtex		2	1										
Virtex2		2	1										
Virtex2p		2	1										
VirtexE		2	1										
Virtex4		2	1										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1										
ECP		2	1										
ECP2		2	1										
ECP2M		2	1										
SC		2	1										
MACHXO		2	1										
XP		2	1										
XP2		2	1										

XOR5B

5-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XOR5N1B

5-Input Exclusive-OR Gate with Active Low A Input, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XOR5N1S

5-Input Exclusive-OR Gate with Active Low A Input, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XOR5N2B

5-Input Exclusive-OR Gate with Active Low A and B Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XOR5N2S

5-Input Exclusive-OR Gate with Active Low A and B Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XOR5N3B

5-Input Exclusive-OR Gate with Active Low A, B and C Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XOR5N3S

5-Input Exclusive-OR Gate with Active Low A, B and C Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XOR5N4B

5-Input Exclusive-OR Gate with Active Low A, B, C and D Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XOR5N4S

5-Input Exclusive-OR Gate with Active Low A, B, C and D Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XOR5N5B

5-Input Exclusive-OR Gate with Active Low A, B, C, D and E Inputs, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XOR5N5S

5-Input Exclusive-OR Gate with Active Low A, B, C, D and E Inputs, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XOR5S

5-Input Exclusive-OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		1	1										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	1												
CoolRunnerXpla3	1												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XOR6B

6-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		5											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XOR6S

6-Input Exclusive-OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		5											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XOR7B

7-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX													
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN													
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		6											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

FPGA Logic Primitive Resource Usage

XOR7S

7-Input Exclusive-OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		6											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

XOR8B

8-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		7											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

XOR8S

8-Input Exclusive-OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		2	2										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		7											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

XOR9B

9-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		8											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

FPGA Logic Primitive Resource Usage

XOR9S

9-Input Exclusive-OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	3										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L		4	3										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		4	3										
Virtex5			2										
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		8											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3										
ECP		4	3										
ECP2		4	3										
ECP2M		4	3										
SC		4	3										
MACHXO		4	3										
XP		4	3										
XP2		4	3										

XOR12B

12-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	3												
CoolRunnerXpla3	3												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		11											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

FPGA Logic Primitive Resource Usage

XOR12S

12-Input Exclusive-OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	3												
CoolRunnerXpla3	3												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		11											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

XOR16B

16-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	5												
CoolRunnerXpla3	5												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		15											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		6	5										
ECP		6	5										
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

FPGA Logic Primitive Resource Usage

XOR16S

16-Input Exclusive-OR Gate, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5			4										
CoolRunner2	5												
CoolRunnerXpla3	5												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		15											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		6	5										
ECP		6	5										
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

XOR32B

32-Input Exclusive-OR Gate, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9										
Cyclone		11	11										
Cyclone2		11	11										
Cyclone3		11	11										
Stratix		11	11										
Stratix2		10	10										
Stratix3			9										
StratixGX		11	11										
Stratix2GX			7										
Max2		11	11										
Max3000a	11	11											
Max7000b	11	11											
Max7000ae	11	11											
Max7000s	11	11											
Spartan2		12	11										
Spartan2E		12	11										
Spartan3		12	11										
Spartan3A		12	11										
Spartan3ADSP		12	11										
Spartan3AN		12	11										
Spartan3E		18	11										
Spartan3L		12	11										
Virtex		12	11										
Virtex2		12	11										
Virtex2p		12	11										
VirtexE		12	11										
Virtex4		12	11										
Virtex5			8										
CoolRunner2	12												
CoolRunnerXpla3	12												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		31											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		12	11										
ECP		12	11										
ECP2		12	11										
ECP2M		12	11										
SC		12	11										
MACHXO		12	11										
XP		12	11										
XP2		12	11										

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1

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