FPGA Latch Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Latch cores.

Core Reference
CR0135 (v1.11) December 19, 2008

Latch

The available Latch cores are listed as follows:

LD	*LD2B*	*LD2CEB*	*LD2CES*
LD2S	*LD3B*	*LD3S*	*LD4B*
LD4CEB	*LD4CES*	*LD4S*	*LD8B*
LD8CEB	*LD8CES*	*LD8S*	*LD16B*
LD16CEB	*LD16CES*	*LD16S*	*LD32B*
LD32CEB	*LD_1*	*LDC*	*LDC_1*
LDCE	*LDCE_1*	*LDCP*	*LDCP_1*
LDCPE	*LDCPE_1*	*LDE*	*LDE_1*
LDP	*LDP_1*	*LDPE*	*LDPE_1*

LD

Transparent Data Latch

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1											
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1											
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1											
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2		1									
ECP		2		1									
ECP2		2	1										
ECP2M		2	1										
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2	1										

LD2B

2-Bit Transparent Data Latch, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2											
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2											
Stratix3			2									1	
StratixGX		2	2									1	
Stratix2GX			2									1	
Max2		2											
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L													
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		4											
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4		2									
ECP		4		2									
ECP2		4	2										
ECP2M		4	2										
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4	2										

LD2CEB

2-Bit Transparent Data Latch with Asynchronous Clear and Gate Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		3	3										
Cyclone2		3	1										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	1										
Stratix3			3									1	
StratixGX		3	3										
Stratix2GX			3									1	
Max2		3	1										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L													
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		6	1										
Virtex5		4	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		6	1	2									
ECP		6	1	2									
ECP2		4	3										
ECP2M		4	3										
SC		6	1	2									
MACHXO		6	1										
XP		6	1	2									
XP2		4	3										

LD2CES

2-Bit Transparent Data Latch with Asynchronous Clear and Gate Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		3	3										
Cyclone2		3	1										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	1										
Stratix3			3									1	
StratixGX		3	3									1	
Stratix2GX			3									1	
Max2		3	1										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		4	3										
Spartan3ADSP		4	3										
Spartan3AN		4	3										
Spartan3E		4	3										
Spartan3L													
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		6	1										
Virtex5		4	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		6	1	2									
ECP		6	1	2									
ECP2		4	3										
ECP2M		4	3										
SC		6	1	2									
MACHXO		6	1										
XP		6	1	2									
XP2		4	3										

LD2S

2-Bit Transparent Data Latch, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2											
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2											
Stratix3			2									1	
StratixGX		2	2									1	
Stratix2GX			2									1	
Max2		2											
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		4											
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4		2									
ECP		4		2									
ECP2		4	2										
ECP2M		4	2										
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4	2										

LD3B

3-Bit Transparent Data Latch, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		3	3										
Cyclone2		3											
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3											
Stratix3			3									1	
StratixGX		3	3									1	
Stratix2GX			3									1	
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3	3										
Spartan3ADSP		3	3										
Spartan3AN		3	3										
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		6											
Virtex5		3	3										
CoolRunner2	3			3									
CoolRunnerXpla3	3			3									
Xc9500	6												
Xc9500XL	6												
Xc9500XV	6												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		6		3									
ECP		6		3									
ECP2		6	3										
ECP2M		6	3										
SC		6		3									
MACHXO		6											
XP		6		3									
XP2		6	3										

LD3S

3-Bit Transparent Data Latch, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		3	3										
Cyclone2		3											
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3											
Stratix3			3									1	
StratixGX		3	3									1	
Stratix2GX			3									1	
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3	3										
Spartan3ADSP		3	3										
Spartan3AN		3	3										
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		6											
Virtex5		3	3	3									
CoolRunner2	3			3									
CoolRunnerXpla3	3			3									
Xc9500	6												
Xc9500XL	6												
Xc9500XV	6												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		6		3									
ECP		6		3									
ECP2		6	3										
ECP2M		6	3										
SC		6		3									
MACHXO		6											
XP		6		3									
XP2		6	3										

LD4B

4-Bit Transparent Data Latch, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		4	4										
Cyclone2		4											
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4											
Stratix3			4									1	
StratixGX		4	4									1	
Stratix2GX			4									1	
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		8											
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		8		4									
ECP		8		4									
ECP2		8	4										
ECP2M		8	4										
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8	4										

LD4CEB

4-Bit Transparent Data Latch with Asynchronous Clear and Gate Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5										
Cyclone		5	5										
Cyclone2		5	1										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	1										
Stratix3			5									1	
StratixGX		5	5									1	
Stratix2GX			5									1	
Max2		5	1										
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		10	1										
Virtex5		6	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		10	1	4									
ECP		10	1	4									
ECP2		6	5										
ECP2M		6	5										
SC		10	1	4									
MACHXO		10	1										
XP		10	1	4									
XP2		6	5										

LD4CES

4-Bit Transparent Data Latch with Asynchronous Clear and Gate Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5										
Cyclone		5	5										
Cyclone2		5	1										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	1										
Stratix3			5									1	
StratixGX		5	5									1	
Stratix2GX			5									1	
Max2		5	1										
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		10	1										
Virtex5		6	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		10	1	4									
ECP		10	1	4									
ECP2		6	5										
ECP2M		6	5										
SC		10	1	4									
MACHXO		10	1										
XP		10	1	4									
XP2		6	5										

LD4S

4-Bit Transparent Data Latch, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		4	4										
Cyclone2		4											
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4											
Stratix3			4									1	
StratixGX		4	4									1	
Stratix2GX			4									1	
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		8											
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		8		4									
ECP		8		4									
ECP2		8	4										
ECP2M		8	4										
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8	4										

LD8B

8-Bit Transparent Data Latch, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8										
Cyclone		8	8										
Cyclone2		8											
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8											
Stratix3			8									1	
StratixGX		8	8									1	
Stratix2GX			8									1	
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		16											
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	16												
Xc9500XL	16												
Xc9500XV	16												
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		16		8									
ECP		16		8									
ECP2		16	8										
ECP2M		16	8										
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16	8										

LD8CEB

8-Bit Transparent Data Latch with Asynchronous Clear and Gate Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9										
Cyclone		9	9										
Cyclone2		9	1										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	1										
Stratix3			9									1	
StratixGX		9	9									1	
Stratix2GX			9									1	
Max2		9	1										
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		10	9										
Spartan2E		10	9										
Spartan3		10	9										
Spartan3A		10	9										
Spartan3ADSP		10	9										
Spartan3AN		10	9										
Spartan3E		10	9										
Spartan3L		10	9										
Virtex		10	9										
Virtex2		10	9										
Virtex2p		10	9										
VirtexE		10	9										
Virtex4		18	1										
Virtex5		10	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	16												
Xc9500XL	16												
Xc9500XV	16												
ProAsicPlus		9											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		18	1	8									
ECP		18	1	8									
ECP2		10	9										
ECP2M		10	9										
SC		18	1	8									
MACHXO		18	1										
XP		18	1	8									
XP2		10	9										

LD8CES

8-Bit Transparent Data Latch with Asynchronous Clear and Gate Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9										
Cyclone		9	9										
Cyclone2		9	1										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	1										
Stratix3			9									1	
StratixGX		9	9									1	
Stratix2GX			9									1	
Max2		9	1										
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		10	9										
Spartan2E		10	9										
Spartan3		10	9										
Spartan3A		10	9										
Spartan3ADSP		10	9										
Spartan3AN		10	9										
Spartan3E		10	9										
Spartan3L		10	9										
Virtex		10	9										
Virtex2		10	9										
Virtex2p		10	9										
VirtexE		10	9										
Virtex4		18	1										
Virtex5		10	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	16												
Xc9500XL	16												
Xc9500XV	16												
ProAsicPlus		9											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		18	1	8									
ECP		18	1	8									
ECP2		10	9										
ECP2M		10	9										
SC		18	1	8									
MACHXO		18	1										
XP		18	1	8									
XP2		10	9										

LD8S

8-Bit Transparent Data Latch, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8										
Cyclone		8	8										
Cyclone2		8											
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8											
Stratix3			8									1	
StratixGX		8	8									1	
Stratix2GX			8									1	
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		16											
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	16												
Xc9500XL	16												
Xc9500XV	16												
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		16		8									
ECP		16		8									
ECP2		16	8										
ECP2M		16	8										
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16	8										

LD16B

16-Bit Transparent Data Latch, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16										
Cyclone		16	16										
Cyclone2		16											
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16											
Stratix3			16									1	
StratixGX		16	16									1	
Stratix2GX			16									1	
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16	16										
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16										
Spartan3L													
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		32											
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	32												
Xc9500XL	32												
Xc9500XV	32												
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		17											
Fusion		16											
EC		32		16									
ECP		32		16									
ECP2		32	16										
ECP2M		32	16										
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32	16										

LD16CEB

16-Bit Transparent Data Latch with Asynchronous Clear and Gate Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17										
Cyclone		17	17										
Cyclone2		17	1										
Cyclone3		17	17										
Stratix		17	17										
Stratix2		17	1										
Stratix3			17									1	
StratixGX		17	17									1	
Stratix2GX			17									1	
Max2		17	1										
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		18	17										
Spartan2E		18	17										
Spartan3		18	17										
Spartan3A		18	17										
Spartan3ADSP		18	17										
Spartan3AN		18	17										
Spartan3E		18	17										
Spartan3L													
Virtex		18	17										
Virtex2		18	17										
Virtex2p		18	17										
VirtexE		18	17										
Virtex4		34	1										
Virtex5		18	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	32												
Xc9500XL	32												
Xc9500XV	32												
ProAsicPlus		17											
ProAsic3		17											
ProAsic3E		19											
Fusion		17											
EC		34	1	16									
ECP		34	1	16									
ECP2		18	17										
ECP2M		18	17										
SC		34	1	16									
MACHXO		34	1										
XP		34	1	16									
XP2		18	17										

LD16CES

16-Bit Transparent Data Latch with Asynchronous Clear and Gate Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17										
Cyclone		17	17										
Cyclone2		17	1										
Cyclone3		17	17										
Stratix		17	17										
Stratix2		17	1										
Stratix3			17									1	
StratixGX		17	17									1	
Stratix2GX			17									1	
Max2		17	1										
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		18	17										
Spartan2E		18	17										
Spartan3		18	17										
Spartan3A		18	17										
Spartan3ADSP		18	17										
Spartan3AN		18	17										
Spartan3E		18	17										
Spartan3L													
Virtex		18	17										
Virtex2		18	17										
Virtex2p		18	17										
VirtexE		18	17										
Virtex4		34	1										
Virtex5		18	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	32												
Xc9500XL	32												
Xc9500XV	32												
ProAsicPlus		17											
ProAsic3		17											
ProAsic3E		19											
Fusion		17											
EC		34	1	16									
ECP		34	1	16									
ECP2		18	17										
ECP2M		18	17										
SC		34	1	16									
MACHXO		34	1										
XP		34	1	16									
XP2		18	17										

LD16S

16-Bit Transparent Data Latch, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16										
Cyclone		16	16										
Cyclone2		16											
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16											
Stratix3			16									1	
StratixGX		16	16									1	
Stratix2GX			16									1	
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16	16										
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16										
Spartan3L													
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		32											
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	32												
Xc9500XL	32												
Xc9500XV	32												
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		17											
Fusion		16											
EC		32		16									
ECP		32		16									
ECP2		32	16										
ECP2M		32	16										
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32	16										

LD32B

32-Bit Transparent Data Latch, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32										
Cyclone		32	32										
Cyclone2		32											
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32											
Stratix3			32									1	
StratixGX		32	32									1	
Stratix2GX			32									1	
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32	32										
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		64											
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		32											
ProAsic3		34											
ProAsic3E		34											
Fusion		32											
EC		64		32									
ECP		64		32									
ECP2		64	32										
ECP2M		64	32										
SC		64		32									
MACHXO		64											
XP		64		32									
XP2		64	32										

LD32CEB

32-Bit Transparent Data Latch with Asynchronous Clear and Gate Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			33										
Cyclone		33	33										
Cyclone2		34	2										
Cyclone3		33	33										
Stratix		33	33										
Stratix2		33	1										
Stratix3			34									2	
StratixGX		33	33									1	
Stratix2GX			34									2	
Max2		33	1										
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		34	33									1	
Spartan2E		34	33									1	
Spartan3		34	33									1	
Spartan3A		34	33										
Spartan3ADSP		34	33										
Spartan3AN		34	33										
Spartan3E		34	33									1	
Spartan3L		34	33										
Virtex		34	33									1	
Virtex2		34	33									1	
Virtex2p		34	33									1	
VirtexE		34	33									1	
Virtex4		66	1										
Virtex5		34	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	64			32									
Xc9500XL	64			32									
Xc9500XV	64			32									
ProAsicPlus		33											
ProAsic3		36											
ProAsic3E		37											
Fusion		33											
EC		66	1	32									
ECP		66	1	32									
ECP2		64	33										
ECP2M		64	33										
SC		66	1	32									
MACHXO		66	1										
XP		66	1	32									
XP2		64	33										

LD_1

Transparent Data Latch with Inverted Gate

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		2	1										
Cyclone3		2	2										
Stratix		1	1										
Stratix2		2	1										
Stratix3			2										
StratixGX		1	1										
Stratix2GX			2										
Max2		2	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2		1									
ECP		2		1									
ECP2		2	1										
ECP2M		2	1										
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2	1										

LDC

Transparent Data Latch with Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1											
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1											
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1											
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2		1									
ECP		2		1									
ECP2		2	1										
ECP2M		2	1										
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2	1										

LDC_1

Transparent Data Latch with Asynchronous Clear and Inverted Gate

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		2	1										
Cyclone3		2	2										
Stratix		1	1										
Stratix2		2	1										
Stratix3			2										
StratixGX		1	1										
Stratix2GX			2										
Max2		2	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2		1									
ECP		2		1									
ECP2		2	1										
ECP2M		2	1										
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2	1										

LDCE

Transparent Data Latch with Asynchronous Clear and Gate Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	1										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	1										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2													
CoolRunnerXpla3													
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4	1	1									
ECP		4	1	1									
ECP2		2	2										
ECP2M		2	2										
SC		4	1	1									
MACHXO		4	1										
XP		4	1	1									
XP2		2	2										

LDCE_1

Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	1										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	1										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2													
CoolRunnerXpla3													
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4	1	1									
ECP		4	1	1									
ECP2		2	2										
ECP2M		2	2										
SC		4	1	1									
MACHXO		4	1										
XP		4	1	1									
XP2		2	2										

LDCP

Transparent Data Latch with Asynchronous Clear and Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	1										
Cyclone2		2											
Cyclone3		2	2										
Stratix		2	1										
Stratix2		1											
Stratix3			1										
StratixGX		2	2										
Stratix2GX			1										
Max2		2											
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2											
Spartan2E		2											
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		2											
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		2											
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		6	3	2									
ECP		6	3	2									
ECP2		4	4										
ECP2M		4	4										
SC		6	2	3									
MACHXO		6	3										
XP		6	3	2									
XP2		4	4										

LDCP_1

Transparent Data Latch with Asynchronous Clear and Preset and Inverted Gate

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		2	1										
Cyclone2		3	1										
Cyclone3		3	3										
Stratix		2	1										
Stratix2		2	1										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		3	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		2											
Spartan2E		2											
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		2											
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		2											
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		6	3	2									
ECP		6	3	2									
ECP2		4	4										
ECP2M		4	4										
SC		6	2	3									
MACHXO		6	3										
XP		6	3	2									
XP2		4	4										

LDCPE

Transparent Data Latch with Asynchronous Clear and Preset and Gate Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	2										
Cyclone2		3	1										
Cyclone3		3	3										
Stratix		3	2										
Stratix2		2	1										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	1										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2											
Spartan2E		2											
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		2											
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		2											
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		8	4	2									
ECP		8	4	2									
ECP2		6	5										
ECP2M		6	5										
SC		8	3	3									
MACHXO		8	4										
XP		8	4	2									
XP2		6	5										

LDCPE_1

Transparent Data Latch with Asynchronous Clear and Preset, Gate Enable, and Inverted Gate

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		3	2										
Cyclone2		3	1										
Cyclone3		3	3										
Stratix		3	2										
Stratix2		2	1										
Stratix3			2										
StratixGX		3	3										
Stratix2GX			2										
Max2		3	1										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2											
Spartan2E		2											
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		2											
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		2											
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		8	4	2									
ECP		8	4	2									
ECP2		6	5										
ECP2M		6	5										
SC		8	3	3									
MACHXO		8	4										
XP		8	4	2									
XP2		6	5										

LDE

Transparent Data Latch with Gate Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	1										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	1										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4	1	1									
ECP		4	1	1									
ECP2		2	1										
ECP2M		2	1										
SC		4	1	1									
MACHXO		4	1										
XP		4	1	1									
XP2		2	1										

LDE_1

Transparent Data Latch with Gate Enable and Inverted Gate

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	1										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	1										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4	1	1									
ECP		4	1	1									
ECP2		2	1										
ECP2M		2	1										
SC		4	1	1									
MACHXO		4	1										
XP		4	1	1									
XP2		2	1										

LDP

Transparent Data Latch with Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		1											
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1											
Stratix3			1										
StratixGX		1	1										
Stratix2GX			1										
Max2		1											
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1												
Xc9500XL	1												
Xc9500XV	1												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2		1									
ECP		2		1									
ECP2		2	1										
ECP2M		2	1										
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2	1										

LDP_1

Transparent Data Latch with Asynchronous Preset and Inverted Gate

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1										
Cyclone		1	1										
Cyclone2		2	1										
Cyclone3		2	2										
Stratix		1	1										
Stratix2		2	1										
Stratix3			2										
StratixGX		1	1										
Stratix2GX			2										
Max2		2	1										
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion		1											
EC		2		1									
ECP		2		1									
ECP2		2	1										
ECP2M		2	1										
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2	1										

LDPE

Transparent Data Latch with Asynchronous Preset and Gate Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	1										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	1										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	1										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2													
CoolRunnerXpla3													
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4	1	1									
ECP		4	1	1									
ECP2		2	2										
ECP2M		2	2										
SC		4	1	1									
MACHXO		4	1										
XP		4	1	1									
XP2		2	2										

LDPE_1

Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	1										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	1										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	1										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1	1										
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1									1	
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		2											
Virtex5		1	1	1									
CoolRunner2													
CoolRunnerXpla3													
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4	1	1									
ECP		4	1	1									
ECP2		2	2										
ECP2M		2	2										
SC		4	1	1									
MACHXO		4	1										
XP		4	1	1									
XP2		2	2										

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1