



FPGA Instruments Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Instruments cores.

Core Reference
CR0134 (v1.10) July 17, 2008

Instruments

The available Instruments cores are listed as follows:

<i>CLKGEN</i>	<i>FRQCNT2</i>	<i>IOB_1X8</i>	<i>IOB_1X16</i>
<i>IOB_2X8</i>	<i>IOB_2X16</i>	<i>IOB_4X8</i>	<i>IOB_4X16</i>
<i>LAX_1K8</i>	<i>LAX_1K16</i>	<i>LAX_2K8</i>	<i>LAX_2K16</i>
<i>LAX_4K8</i>	<i>LAX_4K16</i>	<i>LAX_8</i>	<i>LAX_16</i>
<i>TERMINAL</i>			

FPGA Instruments Resource Usage

CLKGEN

Frequency Generator

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		261	191	224									8
Cyclone2		205	203	226									15
Cyclone3		224	137	224									
Stratix		261	191	224									15
Stratix2		204	202	224									15
StratixGX		260	191	224									15
Max2		263	191	226									4
Max3000a	286	286		224									
Max7000b	286	286		224									
Max7000ae	286	286		224									
Max7000s	298	298		224									
Spartan2		346	228	225									
Spartan2E		346	228	225									
Spartan3		364	236	225									
Spartan3A		559	442	225									
Spartan3E		571	448	225									
Spartan3L		559	442	225									
Virtex		346	228	225									
Virtex2		346	230	225									
Virtex2p		346	230	225									
VirtexE		346	228	225									
Virtex4		589	461	225									
Virtex5		193	193	193									
CoolRunner2	267			224									
CoolRunnerXpla3	756			224									
Xc9500	282			224									
Xc9500XL	260			224									
Xc9500XV	283			224									
ProAsicPlus		803											
ProAsic3		643											
ProAsic3E		650											
EC		366	260	224									
ECP		366	260	224									
ECP2		398	257	224									
ECP2M		398	257	224									
MACHXO		408	276										
XP		394	256	224									
SC		332	256	224									

FRQCNT2

Frequency Counter

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		591	424	544									8
Cyclone2		676	417	415									11
Stratix		591	424	544									9
Stratix2		411	408	412									11
StratixGX		591	424	544									9
Max2		585	418	415									4
Spartan2		696	322	546									
Spartan2E		696	322	545									
Spartan3		690	378	413									
Spartan3A		1085	782	413									
Spartan3E		1108	793	414									
Spartan3L		1085	782	413									
Virtex		696	322	546									
Virtex2		696	325	546									
Virtex2p		696	325	546									
VirtexE		696	322	546									
Virtex4		1102	792	414									
Virtex5		349	349	349									
CoolRunner2	2686												
CoolRunnerXpla3	1536												
ProAsicPlus		1589											
ProAsic3		1368											
ProAsic3E		1382											
EC		1012	577	481									
ECP		1012	577	481									
ECP2		1082	643	483									
ECP2M		1082	643	483									
MACHXO		952	515										
XP		952	510	483									
SC		1064	573	547									

FPGA Instruments Resource Usage

IOB_1X8

1 Ch x 8 Bit Digital IO

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		93	55	77									2
Cyclone2		54	53	78									2
Cyclone3		77	35	77									
Stratix		93	55	77									2
Stratix2		48	47	77									2
StratixGX		93	55	77									2
Max2		95	54	78									2
Max3000a	84	84		77									
Max7000b	84	84		77									
Max7000ae	84	84		77									
Max7000s	84	84		77									
Spartan2		110	93	70									
Spartan2E		110	93	70									
Spartan3		106	90	70									
Spartan3A		166	149	70									
Spartan3E		170	153	70									
Spartan3L		166	149	70									
Virtex		110	93	70									
Virtex2		110	93	70									
Virtex2p		110	93	70									
VirtexE		110	93	70									
Virtex4		192	160	78									
Virtex5		8	8	8									
CoolRunner2	78			77									
CoolRunnerXpla3	78			77									
Xc9500	78			77									
Xc9500XL	78			77									
Xc9500XV	78			77									
ProAsicPlus		250											
ProAsic3		189											
ProAsic3E		190											
EC		118	84	77									
ECP		118	84	77									
ECP2		114	79	77									
ECP2M		114	79	77									
MACHXO		118	80										
XP		116	79	77									
SC		112	79	77									

IOB_1X16

1 Ch x 16 Bit Digital IO

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		109	63	93								2	
Cyclone2		62	61	94								2	
Cyclone3		93	35	93									
Stratix		108	62	93								2	
Stratix2		56	55	93								2	
StratixGX		108	62	93								2	
Max2		110	62	94								2	
Max3000a	100	100		93									
Max7000b	100	100		93									
Max7000ae	100	100		93									
Max7000s	100	100		93									
Spartan2		128	111	78									
Spartan2E		128	111	78									
Spartan3		122	106	78									
Spartan3A		182	165	78									
Spartan3E		184	167	78									
Spartan3L		182	165	78									
Virtex		128	111	78									
Virtex2		128	111	78									
Virtex2p		128	111	78									
VirtexE		128	111	78									
Virtex4		232	184	94									
Virtex5		16	16	16									
CoolRunner2	94			93									
CoolRunnerXpla3	94			93									
Xc9500	94			93									
Xc9500XL	94			93									
Xc9500XV	94			93									
ProAsicPlus		290											
ProAsic3		214											
ProAsic3E		217											
EC		142	92	93									
ECP		142	92	93									
ECP2		138	87	93									
ECP2M		138	87	93									
MACHXO		138	88										
XP		140	87	93									
SC		136	87	93									

FPGA Instruments Resource Usage

IOB_2X8

2 Ch x 8 Bit Digital IO

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		112	67	93								2	
Cyclone2		65	64	94								2	
Cyclone3		93	38	93									
Stratix		112	67	93								2	
Stratix2		59	58	93								2	
StratixGX		112	67	93								2	
Max2		111	65	94								2	
Max3000a	103	103		93									
Max7000b	103	103		93									
Max7000ae	103	103		93									
Max7000s	103	103		93									
Spartan2		128	112	78									
Spartan2E		128	112	78									
Spartan3		124	108	78									
Spartan3A		184	167	78									
Spartan3E		188	171	78									
Spartan3L		184	167	78									
Virtex		128	112	78									
Virtex2		130	114	78									
Virtex2p		130	114	78									
VirtexE		128	112	78									
Virtex4		234	186	94									
Virtex5		16	16	16									
CoolRunner2	94			93									
CoolRunnerXpla3	94			93									
Xc9500	94			93									
Xc9500XL	94			93									
Xc9500XV	94			93									
ProAsicPlus		296											
ProAsic3		216											
ProAsic3E		218											
EC		146	95	93									
ECP		146	95	93									
ECP2		144	89	93									
ECP2M		144	89	93									
MACHXO		144	90										
XP		144	89	93									
SC		138	89	93									

IOB_2X16

2 Ch x 16 Bit Digital IO

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		143	83	125									2
Cyclone2		82	81	126									2
Cyclone3		125	38	125									
Stratix		143	83	125									2
Stratix2		76	75	125									2
StratixGX		143	83	125									2
Max2		143	81	126									2
Max3000a	135	135		125									
Max7000b	135	135		125									
Max7000ae	135	135		125									
Max7000s	135	135		125									
Spartan2		162	145	94									
Spartan2E		162	145	94									
Spartan3		160	142	94									
Spartan3A		216	199	94									
Spartan3E		220	203	94									
Spartan3L		216	199	94									
Virtex		162	145	94									
Virtex2		164	147	94									
Virtex2p		164	147	94									
VirtexE		162	145	94									
Virtex4		316	236	126									
Virtex5		32	32	32									
CoolRunner2	126			125									
CoolRunnerXpla3	126			125									
Xc9500	126			125									
Xc9500XL	126			125									
Xc9500XV	126			125									
ProAsicPlus		376											
ProAsic3		266											
ProAsic3E		271											
EC		194	111	125									
ECP		194	111	125									
ECP2		192	105	125									
ECP2M		192	105	125									
MACHXO		194	108										
XP		192	105	125									
SC		186	105	125									

FPGA Instruments Resource Usage

IOB_4X8

4 Ch x 8 Bit Digital IO

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		147	88	125									2
Cyclone2		88	87	126									2
Cyclone3		125	42	125									
Stratix		147	88	125									2
Stratix2		83	82	125									2
StratixGX		147	88	125									2
Max2		149	88	126									2
Max3000a	139	139		125									
Max7000b	139	139		125									
Max7000ae	139	139		125									
Max7000s	139	139		125									
Spartan2		164	148	94									
Spartan2E		164	148	94									
Spartan3		162	145	94									
Spartan3A		222	204	94									
Spartan3E		224	208	94									
Spartan3L		222	204	94									
Virtex		164	148	94									
Virtex2		164	148	94									
Virtex2p		164	148	94									
VirtexE		164	148	94									
Virtex4		320	239	126									
Virtex5		32	32	32									
CoolRunner2	126			125									
CoolRunnerXpla3	126			125									
Xc9500	126			125									
Xc9500XL	126			125									
Xc9500XV	126			125									
ProAsicPlus		384											
ProAsic3		275											
ProAsic3E		277											
EC		208	119	125									
ECP		208	119	125									
ECP2		202	110	125									
ECP2M		202	110	125									
MACHXO		200	112										
XP		202	110	125									
SC		194	110	125									

IOB_4X16

4 Ch x 16 Bit Digital IO

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		212	121	189									2
Cyclone2		120	119	190									2
Cyclone3		189	42	189									
Stratix		212	121	189									2
Stratix2		117	116	189									2
StratixGX		212	121	189									2
Max2		223	120	190									1
Max3000a	203	203		189									
Max7000b	203	203		189									
Max7000ae	203	203		189									
Max7000s	203	203		189									
Spartan2		240	214	127									
Spartan2E		240	214	126									
Spartan3		236	210	126									
Spartan3A		298	272	126									
Spartan3E		295	274	127									
Spartan3L		296	268	126									
Virtex		240	214	127									
Virtex2		234	214	127									
Virtex2p		234	214	127									
VirtexE		240	214	127									
Virtex4		489	337	191									
Virtex5		64	64	64									
CoolRunner2	190			189									
CoolRunnerXpla3	190			189									
Xc9500	190			189									
Xc9500XL	190			189									
Xc9500XV	190			189									
ProAsicPlus		544											
ProAsic3		375											
ProAsic3E		385											
EC		310	151	195									
ECP		310	151	195									
ECP2		306	142	197									
ECP2M		306	142	197									
MACHXO		308	147										
XP		306	144	197									
SC		300	145	197									

FPGA Instruments Resource Usage

LAX_1K8

Logic Analyzer 1K8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		609	535	330		2							4
Cyclone2		530	530	332		2							4
Cyclone3		421	421	353									
Stratix		613	538	330		2							4
Stratix2		462	463	330		2							4
StratixGX		614	539	330		2							4
Spartan2		677	512	321		2							1
Spartan2E		691	512	320		2							1
Spartan3		661	505	320	1								1
Spartan3A		1055	877	347									
Spartan3E		1186	1021	348	1								
Spartan3L		1025	855	343									
Virtex		681	514	321		2							1
Virtex2		673	511	321	1								1
Virtex2p		673	512	321	1								1
VirtexE		681	512	321		2							1
Virtex5		11	11	11									
ProAsicPlus		1816						4					
ProAsic3		1679				2							
ProAsic3E		1708					2						
EC		900	763	344			1						
ECP		900	763	344			1						
MACHXO		932	792				1						
XP		980	793	363			1						
SC		904	756	368			1						

LAX_1K16

Logic Analyzer 1K16

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		765	653	426		4							4
Cyclone2		657	657	428		4							4
Cyclone3		482	482	457									
Stratix		768	655	426		4							4
Stratix2		573	574	426		4							4
StratixGX		769	656	426		4							4
Spartan2		837	629	410		4							1
Spartan2E		843	633	409		4							1
Spartan3		831	627	408	1								1
Spartan3A		1314	1079	444									
Spartan3E		1479	1251	445	1								
Spartan3L		1290	1068	440									
Virtex		847	634	410		4							1
Virtex2		845	633	410	1								1
Virtex2p		845	633	410	1								1
VirtexE		837	626	410		4							1
Virtex4		1244	1032	428	1								
Virtex5		19	19	19									
ProAsicPlus		2360						8					
ProAsic3		2204				4							
ProAsic3E		2246						4					
EC		1146	961	449			2						
ECP		1146	961	449			2						
MACHXO		1190	1023				2						
XP		1230	1024	466			2						
SC		1154	956	480			1						

FPGA Instruments Resource Usage

LAX_2K8

Logic Analyzer 2K8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		628	555	336		4							4
Cyclone2		548	548	338		4							4
Cyclone3		413	413	359									
Stratix		625	551	336		4							4
Stratix2		473	474	336		4							4
StratixGX		626	552	336		4							4
Spartan2		685	526	327		4							1
Spartan2E		701	524	326		4							1
Spartan3		667	511	326	1								1
Spartan3A		1054	880	354									
Spartan3E		1177	1012	355	1								
Spartan3L		1040	869	350									
Virtex		679	518	327		4							1
Virtex2		681	522	327	1								1
Virtex2p		681	522	327	1								1
VirtexE		681	524	327		4							1
Virtex4		992	838	338	1								
Virtex5		11	11	11									
ProAsicPlus		1878						8					
ProAsic3		1713				4							
ProAsic3E		1740					4						
EC		926	782	350			2						
ECP		926	782	350			2						
MACHXO		952	823				2						
XP		1002	824	371			2						
SC		914	776	375			1						

LAX_2K16

Logic Analyzer 2K16

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		767	654	432		8							4
Cyclone2		665	665	434		8							4
Cyclone3		494	494	463									
Stratix		813	701	432		8							4
Stratix2		594	595	432		8							4
StratixGX		814	702	432		8							4
Spartan2		857	650	416		8							1
Spartan2E		855	648	416		8							1
Spartan3		853	639	414	2								1
Spartan3A		1310	1082	450									
Spartan3E		1387	1161	451	2								
Spartan3L		1316	1086	446									
Virtex		859	652	416		8							1
Virtex2		877	658	416	2								1
Virtex2p		877	658	416	2								1
VirtexE		857	649	416		8							1
Virtex4		1272	1056	434	2								
Virtex5		19	19	19									
ProAsicPlus		2437						16					
ProAsic3		2251				8							
ProAsic3E		2296						8					
EC		1178	981	456			4						
ECP		1178	981	456			4						
MACHXO		1224	1051				4						
XP		1274	1052	476			4						
SC		1174	981	484			2						

FPGA Instruments Resource Usage

LAX_4K8

Logic Analyzer 4K8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		627	552	342		8							4
Cyclone2		551	551	344		8							4
Cyclone3		439	439	365									
Stratix		638	563	342		8							4
Stratix2		468	469	342		8							4
StratixGX		639	564	342		8							4
Spartan2		699	535	333		8							1
Spartan2E		715	530	332		8							1
Spartan3		687	525	332	2								1
Spartan3A		1048	872	360									
Spartan3E		1283	1113	361	2								
Spartan3L		1076	903	356									
Virtex		697	534	333		8							1
Virtex2		697	532	333	2								1
Virtex2p		697	532	333	2								1
VirtexE		691	529	333		8							1
Virtex4		1014	858	344	2								
Virtex5		11	11	11									
ProAsicPlus		1961						16					
ProAsic3		1756				8							
ProAsic3E		1791					8						
EC		936	795	356			4						
ECP		936	795	356			4						
MACHXO		978	837				4						
XP		1028	838	376			4						
SC		946	783	380			2						

LAX_4K16

Logic Analyzer 4K16

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		782	668	438		16							4
Cyclone2		676	676	440		16							4
Cyclone3		515	515	469									
Stratix		799	684	438		16							4
Stratix2		616	617	438		16							4
StratixGX		800	685	438		16							4
Spartan2		869	656	422		16							1
Spartan2E		859	647	422		16							1
Spartan3		865	655	420	4								1
Spartan3A		1322	1095	456									
Spartan3E		1473	1240	457	4								
Spartan3L		1328	1098	452									
Virtex		865	656	422		16							1
Virtex2		869	653	422	4								1
Virtex2p		869	653	422	4								1
VirtexE		863	651	422		16							1
Virtex4		1282	1070	440	4								
Virtex5		19	19	19									
ProAsicPlus		2584						32					
ProAsic3		2297				16							
ProAsic3E		2344						16					
EC		1192	995	462			8						
ECP		1192	995	462			8						
MACHXO		1230	1054				8						
XP		1272	1055	480			8						
SC		1202	999	490			4						

FPGA Instruments Resource Usage

LAX_8

Logic Analyzer 8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		768	699	412									4
Cyclone2		693	694	413									4
Cyclone3		590	590	434									
Stratix		770	700	412									4
Stratix2		598	599	411									4
StratixGX		769	700	412									4
Spartan2		877	655	387									1
Spartan2E		857	646	387									1
Spartan3		845	627	385									1
Spartan3A		1301	1074	413									
Spartan3E		1398	1176	414									
Spartan3L		1287	1063	409									
Virtex		867	649	387									1
Virtex2		885	661	387									1
Virtex2p		871	649	387									1
VirtexE		869	646	387									1
Virtex4		1237	1012	413									
Virtex5		27	27	27									
ProAsicPlus		2374											
ProAsic3		2236											
ProAsic3E		2267											
EC		1206	1013	441									
ECP		1206	1013	441									
ECP2		990	708	465									
ECP2M		990	708	465									
MACHXO		1228	1055										
XP		1192	952	453									
SC		1172	990	461									

LAX_16

Logic Analyzer 16

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		926	818	508									4
Cyclone2		813	814	509									4
Cyclone3		672	672	538									
Stratix		945	836	508									4
Stratix2		726	727	507									4
StratixGX		945	836	508									4
Spartan2		1053	788	459									1
Spartan2E		1039	784	459									1
Spartan3		1031	770	457									1
Spartan3A		1505	1235	493									
Spartan3E		1634	1356	494									
Spartan3L		1513	1240	489									
Virtex		1039	786	459									1
Virtex2		1065	807	459									1
Virtex2p		1065	805	459									1
VirtexE		1039	784	459									1
Virtex4		1493	1214	509									
Virtex5		51	51	51									
ProAsicPlus		2930											
ProAsic3		2793											
ProAsic3E		2840											
EC		1436	1212	522									
ECP		1436	1212	522									
ECP2		1188	841	557									
ECP2M		1188	841	557									
MACHXO		1484	1270										
XP		1430	1143	540									
SC		1454	1217	567									

FPGA Instruments Resource Usage

TERMINAL

Instrument Terminal (Wishbone)

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone		167		116									
Cyclone2		116	112	116									
Cyclone3		116	113	116									
Spartan2		277	236	109									
Spartan2E		277	236	109									
Spartan3		275	235	109									
Spartan3A		275	235	109									
Virtex		277	236	109									
Virtex2		275	235	109									
Virtex2p		275	235	109									
VirtexE		277	236	109									
Virtex4		275	235	109									
Virtex5		8	8	8									
ProAsicPlus		397								2			
ProAsic3		309											
EC		180	126	116									
ECP		180	126	116									
ECP2		180	126	116									
ECP2M		180	126	116									
SC		166	126	116									
XP		180	126	116									
MACHXO		168	126										

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
29-Dec-2005	1.04	Added ProAsic3
20-Apr-2006	1.05	Tools Utilized section added
15-Jun-2006	1.06	Proasic3E and XP added
31-Jul-2006	1.07	MACHXO added
1-May-2007	1.08	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added.
4-Jul-2007	1.09	Terminal And configurable DIGITAL IO Core added.
17-Jul-2008	1.10	Altium Designer Summer 08 SP1

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