FPGA Flip-Flop Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Flip-Flop cores.

Core Reference
CR0133 (v1.11) December 19, 2008

Flip-Flop

The available Flip-Flop cores are listed as follows:

FD	*FD2B*	*FD2CB*	*FD2CEB*
FD2CES	*FD2CPB*	*FD2CPEB*	*FD2CPES*
FD2CPS	*FD2CS*	*FD2EB*	*FD2ES*
FD2PB	*FD2PEB*	*FD2PES*	*FD2PS*
FD2RB	*FD2REB*	*FD2RES*	*FD2RS*
FD2RSB	*FD2RSEB*	*FD2RSES*	*FD2RSS*
FD2S	*FD2SB*	*FD2SEB*	*FD2SES*
FD2SRB	*FD2SREB*	*FD2SRES*	*FD2SRS*
FD2SS	*FD4B*	*FD4CB*	*FD4CEB*
FD4CES	*FD4CPB*	*FD4CPEB*	*FD4CPES*
FD4CPS	*FD4CS*	*FD4EB*	*FD4ES*
FD4PB	*FD4PEB*	*FD4PES*	*FD4PS*
FD4RB	*FD4REB*	*FD4RES*	*FD4RS*
FD4RSB	*FD4RSEB*	*FD4RSES*	*FD4RSS*
FD4S	*FD4SB*	*FD4SEB*	*FD4SES*
FD4SRB	*FD4SREB*	*FD4SRES*	*FD4SRS*
FD4SS	*FD8B*	*FD8CB*	*FD8CEB*
FD8CES	*FD8CPB*	*FD8CPEB*	*FD8CPES*
FD8CPS	*FD8CS*	*FD8EB*	*FD8ES*
FD8PB	*FD8PEB*	*FD8PES*	*FD8PS*
FD8RB	*FD8REB*	*FD8RES*	*FD8RS*
FD8RSB	*FD8RSEB*	*FD8RSES*	*FD8RSS*
FD8S	*FD8SB*	*FD8SEB*	*FD8SES*
FD8SRB	*FD8SREB*	*FD8SRES*	*FD8SRS*
FD8SS	*FD16B*	*FD16CB*	*FD16CEB*
FD16CES	*FD16CPB*	*FD16CPEB*	*FD16CPES*

FD16CPS
FD16CS
FD16EB
FD16ES
FD16PB
FD16PEB
FD16PES
FD16PS
FD16RB
FD16REB
FD16RES
FD16RS
FD16RSB
FD16RSEB
FD16RSES
FD16RSS
FD16S
FD16SB
FD16SEB
FD16SES
FD16SRB
FD16SREB
FD16SRES
FD16SRS
FD16SS
FD32B
FD32CB
FD32CEB
FD32CPB
FD32CPEB
FD32EB
FD32PB
FD32PEB
FD32RB
FD32REB
FD32RSB
FD32RSEB
FD32SB
FD32SEB
FD32SRB
FD32SREB
FD_1
FDC
FDC_1
FDCE
FDCE_1
FDCEN
FDCN
FDCP
FDCP_1
FDCPE
FDCPE_1
FDCPEN
FDCPN
FDE
FDE_1
FDEN
FDN
FDP
FDP_1
FDPE
FDPE_1
FDPEN
FDPN
FDR
FDR_1
FDRE
FDRE_1
FDREN
FDRN
FDRS
FDRS_1
FDRSE
FDRSE_1
FDRSEN
FDRSN
FDS
FDS_1
FDSE
FDSE_1
FDSEN
FDSN
FDSR
FDSR_1
FDSRE
FDSRE_1
FDSREN
FDSRN
FJKC
FJKC_1
FJKCE
FJKCE_1
FJKCEN
FJKCN
FJKCP
FJKCP_1
FJKCPE
FJKCPE_1
FJKCPEN
FJKCPN
FJKP
FJKP_1
FJKPE
FJKPE_1
FJKPEN
FJKPN
FJKRSE
FJKRSE_1
FJKRSEN
FJKSRE
FJKSRE_1
FJKSREN
FTC
FTC_1
FTCE
FTCE_1
FTCEN
FTCLE
FTCLE_1
FTCLEN
FTCN
FTCP
FTCP_1
FTCPE
FTCPE_1
FTCPEN
FTCPLE
FTCPLE_1
FTCPLEN
FTCPN
FTP
FTP_1
FTPE
FTPE_1
FTPEN
FTPLE
FTPLE_1
FTPLEN
FTPN
FTRSE
FTRSE_1
FTRSEN
FTRSLE
FTRSLE_1
FTRSLEN
FTSRE
FTSRE_1
FTSREN
FTSRLE
FTSRLE_1
FTSRLEN

FD

D-Type Flip-Flop

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				1									
Cyclone		1		1									
Cyclone2				1									
Cyclone3		1		1									
Stratix		1		1									
Stratix2				1									
Stratix3				1									
StratixGX		1		1									
Stratix2GX				1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion													
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FD2B

2-Bit D-Type Flip-Flop, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				2									
Cyclone		2		2								1	
Cyclone2				2									
Cyclone3		2		2									
Stratix		2		2								1	
Stratix2				2									
Stratix3				2								1	
StratixGX		2		2									
Stratix2GX				2								1	
Max2		2		2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion													
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2CB

2-Bit D-Type Flip-Flop with Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				2									
Cyclone		2		2								2	
Cyclone2				2									
Cyclone3		2		2									
Stratix		2		2								2	
Stratix2				2									
Stratix3				2								2	
StratixGX		2		2								2	
Stratix2GX				2								2	
Max2		2		2								2	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion													
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2CEB

2-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				2									
Cyclone		2		2								2	
Cyclone2				2									
Cyclone3		2		2									
Stratix		2		2								2	
Stratix2				2									
Stratix3				2								2	
StratixGX		2		2									
Stratix2GX				2								2	
Max2		2		2								2	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2CES

2-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				2									
Cyclone		2		2								2	
Cyclone2				2									
Cyclone3		2		2									
Stratix		2		2								2	
Stratix2				2									
Stratix3				2								2	
StratixGX		2		2								2	
Stratix2GX				2								2	
Max2		2		2								2	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2CPB

2-Bit D-Type Flip-Flop with Asynchronous Preset and Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				2									
Cyclone		2		2								3	
Cyclone2		6		2									
Cyclone3		6	6	2									
Stratix		2		2								3	
Stratix2				2									
Stratix3			6	2								2	
StratixGX		2		2								3	
Stratix2GX				2								3	
Max2		2		2								3	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		4		2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8	4	3									
ECP		8	4	3									
ECP2		8	3	4									
ECP2M		8	3	4									
SC		10	3	5									
MACHXO		8	4										
XP		8	4	3									
XP2		8	3	4									

FD2CPEB

2-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								3	
Cyclone2		8	2	2									
Cyclone3		8	8	2									
Stratix		2	2	2								3	
Stratix2		2	2	2									
Stratix3			6	2								2	
StratixGX		2	2	2								3	
Stratix2GX			2	2								3	
Max2		4	2	2								3	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		4		2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		10											
ProAsic3		10											
ProAsic3E		10											
Fusion		10											
EC		8	4	3									
ECP		8	4	3									
ECP2		8	5	4									
ECP2M		8	5	4									
SC		10	5	5									
MACHXO		8	4										
XP		8	4	3									
XP2		8	5	4									

FD2CPES

2-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								3	
Cyclone2		8	2	2									
Cyclone3		8	8	2									
Stratix		2	2	2								3	
Stratix2		2	2	2									
Stratix3			6	2								2	
StratixGX		2	2	2								3	
Stratix2GX			2	2								3	
Max2		4	2	2								3	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		4		2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		10											
ProAsic3		10											
ProAsic3E		10											
Fusion		10											
EC		8	4	3									
ECP		8	4	3									
ECP2		8	5	4									
ECP2M		8	5	4									
SC		10	5	5									
MACHXO		8	4										
XP		8	4	3									
XP2		8	5	4									

FD2CPS

2-Bit D-Type Flip-Flop with Asynchronous Preset and Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				2									
Cyclone		2		2								3	
Cyclone2		6		2									
Cyclone3		6	6	2									
Stratix		2		2								3	
Stratix2				2									
Stratix3			6	2								2	
StratixGX		2		2								3	
Stratix2GX				2								3	
Max2		2		2								3	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		4		2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8	4	3									
ECP		8	4	3									
ECP2		8	3	4									
ECP2M		8	3	4									
SC		10	3	5									
MACHXO		8	4										
XP		8	4	3									
XP2		8	3	4									

FD2CS

2-Bit D-Type Flip-Flop with Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				2									
Cyclone		2		2								2	
Cyclone2				2									
Cyclone3		2		2									
Stratix		2		2								2	
Stratix2				2									
Stratix3				2								2	
StratixGX		2		2								2	
Stratix2GX				2								2	
Max2		2		2								2	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion													
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2EB

2-Bit D Flip-Flop with Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				2									
Cyclone		2		2								1	
Cyclone2				2									
Cyclone3		2		2									
Stratix		2		2								1	
Stratix2				2									
Stratix3				2								1	
StratixGX		2		2								1	
Stratix2GX				2								1	
Max2		2		2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion													
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2ES

2-Bit D Flip-Flop with Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				2									
Cyclone		2		2								1	
Cyclone2				2									
Cyclone3		2		2									
Stratix		2		2								1	
Stratix2				2									
Stratix3				2								1	
StratixGX		2		2								1	
Stratix2GX				2								1	
Max2		2		2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion													
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2PB

2-Bit D-Type Flip-Flop with Asynchronous Preset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		4	2	2								2	
Cyclone2		4	2	2									
Cyclone3		4	4	2									
Stratix		4	2	2								2	
Stratix2		4	2	2									
Stratix3			4	2								2	
StratixGX		4	2	2								2	
Stratix2GX			4	2								2	
Max2		4	2	2								2	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion													
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2PEB

2-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		4	2	2								2	
Cyclone2		4	2	2									
Cyclone3		4	4	2									
Stratix		4	2	2								2	
Stratix2		4	2	2									
Stratix3			4	2								2	
StratixGX		4	2	2								2	
Stratix2GX			4	2								2	
Max2		4	2	2								2	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2PES

2-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		4	2	2								2	
Cyclone2		4	2	2									
Cyclone3		4	4	2									
Stratix		4	2	2								2	
Stratix2		4	2	2									
Stratix3			4	2								2	
StratixGX		4	2	2								2	
Stratix2GX			4	2								2	
Max2		4	2	2								2	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2PS

2-Bit D-Type Flip-Flop with Asynchronous Preset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		4	2	2								2	
Cyclone2		4	2	2									
Cyclone3		4	4	2									
Stratix		4	2	2								2	
Stratix2		4	2	2									
Stratix3			4	2								2	
StratixGX		4	2	2								2	
Stratix2GX			4	2								2	
Max2		4	2	2								2	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion													
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2RB

2-Bit D-Type Flip-Flop with Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3			2	2								1	
StratixGX		2	2	2									
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		2											
EC		4	2	2									
ECP		4	2	2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4	2										
XP		4	2	2									
XP2		4		2									

FD2REB

2-Bit D-Type Flip-Flop with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		3	3	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3			2	2								1	
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	2	2									
ECP		4	2	2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4	2										
XP		4	2	2									
XP2		4		2									

FD2RES

2-Bit D-Type Flip-Flop with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		3	3	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3			2	2								1	
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	2	2									
ECP		4	2	2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4	2										
XP		4	2	2									
XP2		4		2									

FD2RS

2-Bit D-Type Flip-Flop with Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3			2	2								1	
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		2											
EC		4	2	2									
ECP		4	2	2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4	2										
XP		4	2	2									
XP2		4		2									

FD2RSB

2-Bit D-Type Flip-Flop with Synchronous Reset and Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3			2	2								1	
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		4		2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		2											
EC		4	2	2									
ECP		4	2	2									
ECP2		4	2	2									
ECP2M		4	2	2									
SC		4	2	2									
MACHXO		4	2										
XP		4	2	2									
XP2		4	2	2									

FD2RSEB

2-Bit D-Type Flip-Flop with Synchronous Reset and Set and Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		4	4	2								1	
Cyclone2		4	4	2									
Cyclone3		3	3	2									
Stratix		4	4	2								1	
Stratix2		2	2	2									
Stratix3			2	2								1	
StratixGX		4	4	2									
Stratix2GX			2	2								1	
Max2		4	4	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		4		2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4	2									
ECP		4	4	2									
ECP2		6	3	2									
ECP2M		6	3	2									
SC		6	3	2									
MACHXO		4	4										
XP		4	4	2									
XP2		6	3	2									

FD2RSES

2-Bit D-Type Flip-Flop with Synchronous Reset and Set and Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		4	4	2								1	
Cyclone2		4	4	2									
Cyclone3		3	3	2									
Stratix		4	4	2								1	
Stratix2		2	2	2									
Stratix3													
StratixGX		4	4	2								1	
Stratix2GX			2	2								1	
Max2		4	4	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		4		2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	4	2									
ECP		4	4	2									
ECP2		6	3	2									
ECP2M		6	3	2									
SC		6	3	2									
MACHXO		4	4										
XP		4	4	2									
XP2		6	3	2									

FD2RSS

2-Bit D-Type Flip-Flop with Synchronous Reset and Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3													
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		4		2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		2											
EC		4	2	2									
ECP		4	2	2									
ECP2		4	2	2									
ECP2M		4	2	2									
SC		4	2	2									
MACHXO		4	2										
XP		4	2	2									
XP2		4	2	2									

FD2S

2-Bit D-Type Flip-Flop, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				2									
Cyclone		2		2								1	
Cyclone2				2									
Cyclone3		2		2									
Stratix		2		2								1	
Stratix2				2									
Stratix3													
StratixGX		2		2								1	
Stratix2GX				2								1	
Max2		2		2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion													
EC		4		2									
ECP		4		2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4											
XP		4		2									
XP2		4		2									

FD2SB

2-Bit D-Type Flip-Flop with Synchronous Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3													
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		2											
EC		4	2	2									
ECP		4	2	2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4	2										
XP		4	2	2									
XP2		4		2									

FD2SEB

2-Bit D-Type Flip-Flop with Clock Enable and Synchronous Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		3	3	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3													
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	2	2									
ECP		4	2	2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4	2										
XP		4	2	2									
XP2		4		2									

FD2SES

2-Bit D-Type Flip-Flop with Clock Enable and Synchronous Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		3	3	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3													
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	2	2									
ECP		4	2	2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4	2										
XP		4	2	2									
XP2		4		2									

FD2SRB

2-Bit D-Type Flip-Flop with Synchronous Set and Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3													
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4	4	2									
Spartan2E		4	4	2									
Spartan3		4	4	2									
Spartan3A		4	4	2									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	2									
Spartan3L		4	4	2									
Virtex		4	4	2									
Virtex2		4	4	2									
Virtex2p		4	4	2									
VirtexE		4	4	2									
Virtex4		4	4	2									
Virtex5		6	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		2											
EC		4	2	2									
ECP		4	2	2									
ECP2		4	2	2									
ECP2M		4	2	2									
SC		4	2	2									
MACHXO		4	2										
XP		4	2	2									
XP2		4	2	2									

FD2SREB

2-Bit D-Type Flip-Flop with Synchronous Set and Reset and Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		4	4	2								1	
Cyclone2		4	4	2									
Cyclone3		3	3	2									
Stratix		4	4	2								1	
Stratix2		2	2	2									
Stratix3													
StratixGX		4	4	2									
Stratix2GX			2	2								1	
Max2		4	4	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		6	5	2									
Spartan2E		6	5	2									
Spartan3		6	5	2									
Spartan3A		6	5	2									
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5	2									
Spartan3L		6	5	2									
Virtex		6	5	2									
Virtex2		6	5	2									
Virtex2p		6	5	2									
VirtexE		6	5	2									
Virtex4		6	5	2									
Virtex5		8	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		9											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		4	4	2									
ECP		4	4	2									
ECP2		6	3	2									
ECP2M		6	3	2									
SC		6	3	2									
MACHXO		6	5										
XP		6	5	2									
XP2		6	3	2									

FD2SRES

2-Bit D-Type Flip-Flop with Synchronous Set and Reset and Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		4	4	2								1	
Cyclone2		4	4	2									
Cyclone3		3	3	2									
Stratix		4	4	2								1	
Stratix2		2	2	2									
Stratix3													
StratixGX		4	4	2								1	
Stratix2GX			2	2								1	
Max2		4	4	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		6	5	2									
Spartan2E		6	5	2									
Spartan3		6	5	2									
Spartan3A		6	5	2									
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5	2									
Spartan3L		6	5	2									
Virtex		6	5	2									
Virtex2		6	5	2									
Virtex2p		6	5	2									
VirtexE		6	5	2									
Virtex4		6	5	2									
Virtex5		6	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		9											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		4	4	2									
ECP		4	4	2									
ECP2		6	3	2									
ECP2M		6	3	2									
SC		6	3	2									
MACHXO		6	5										
XP		6	5	2									
XP2		6	3	2									

FD2SRS

2-Bit D-Type Flip-Flop with Synchronous Set and Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3													
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4	4	2									
Spartan2E		4	4	2									
Spartan3		4	4	2									
Spartan3A		4	4	2									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	2									
Spartan3L		4	4	2									
Virtex		4	4	2									
Virtex2		4	4	2									
Virtex2p		4	4	2									
VirtexE		4	4	2									
Virtex4		4	4	2									
Virtex5		6	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		2											
EC		4	2	2									
ECP		4	2	2									
ECP2		4	2	2									
ECP2M		4	2	2									
SC		4	2	2									
MACHXO		4	2										
XP		4	2	2									
XP2		4	2	2									

FD2SS

2-Bit D-Type Flip-Flop with Synchronous Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								1	
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2								1	
Stratix2		2	2	2									
Stratix3													
StratixGX		2	2	2								1	
Stratix2GX			2	2								1	
Max2		2	2	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		2	2	2									
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2	2									
Spartan3L		2	2	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		2											
EC		4	2	2									
ECP		4	2	2									
ECP2		4		2									
ECP2M		4		2									
SC		4		2									
MACHXO		4	2										
XP		4	2	2									
XP2		4		2									

FD4B

4-Bit D-Type Flip-Flop, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				4									
Cyclone		4		4								1	
Cyclone2				4									
Cyclone3		4		4									
Stratix		4		4								1	
Stratix2				4									
Stratix3													
StratixGX		4		4								1	
Stratix2GX				4								1	
Max2		4		4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion													
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4CB

4-Bit D-Type Flip-Flop with Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				4									
Cyclone		4		4								2	
Cyclone2				4									
Cyclone3		4		4									
Stratix		4		4								2	
Stratix2				4									
Stratix3													
StratixGX		4		4								2	
Stratix2GX				4								2	
Max2		4		4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion													
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4CEB

4-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				4									
Cyclone		4		4								2	
Cyclone2				4									
Cyclone3		4		4									
Stratix		4		4								2	
Stratix2				4									
Stratix3													
StratixGX		4		4									
Stratix2GX				4								2	
Max2		4		4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4CES

4-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				4									
Cyclone		4		4								2	
Cyclone2				4									
Cyclone3		4		4									
Stratix		4		4								2	
Stratix2				4									
Stratix3													
StratixGX		4		4								2	
Stratix2GX				4								2	
Max2		4		4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4CPB

4-Bit D-Type Flip-Flop with Asynchronous Preset and Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				4									
Cyclone		4		4								3	
Cyclone2		10		4									
Cyclone3		10	10	4									
Stratix		4		4								3	
Stratix2				4									
Stratix3													
StratixGX		4		4								3	
Stratix2GX				4								3	
Max2		4		4								3	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		8		4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		12	6	5									
ECP		12	6	5									
ECP2		16	5	8									
ECP2M		16	5	8									
SC		18	5	9									
MACHXO		12	6										
XP		12	6	5									
XP2		16	5	8									

FD4CPEB

4-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								3	
Cyclone2		14	4	4									
Cyclone3		14	14	4									
Stratix		4	4	4								3	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4								3	
Stratix2GX			4	4								3	
Max2		8	4	4								3	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		8		4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		20											
ProAsic3		20											
ProAsic3E		20											
Fusion		20											
EC		12	6	5									
ECP		12	6	5									
ECP2		16	9	8									
ECP2M		16	9	8									
SC		18	9	9									
MACHXO		12	6										
XP		12	6	5									
XP2		16	9	8									

FD4CPES

4-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								3	
Cyclone2		14	4	4									
Cyclone3		14	14	4									
Stratix		4	4	4								3	
Stratix2		4	4	4									
Stratix3													
StratixGX		8	4	4									
Stratix2GX			4	4								3	
Max2		8	4	4								3	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		8		4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		20											
ProAsic3		20											
ProAsic3E		20											
Fusion		20											
EC		12	6	5									
ECP		12	6	5									
ECP2		16	9	8									
ECP2M		16	9	8									
SC		18	9	9									
MACHXO		12	6										
XP		12	6	5									
XP2		16	9	8									

FD4CPS

4-Bit D-Type Flip-Flop with Asynchronous Preset and Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				4									
Cyclone		4		4								3	
Cyclone2		10		4									
Cyclone3		10	10	4									
Stratix		4		4								3	
Stratix2				4									
Stratix3													
StratixGX		4		4								3	
Stratix2GX				4								3	
Max2		4		4								3	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		8		4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		12	6	5									
ECP		12	6	5									
ECP2		16	5	8									
ECP2M		16	5	8									
SC		18	5	9									
MACHXO		12	6										
XP		12	6	5									
XP2		16	5	8									

FD4CS

4-Bit D-Type Flip-Flop with Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				4									
Cyclone		4		4								2	
Cyclone2				4									
Cyclone3		4		4									
Stratix		4		4								2	
Stratix2				4									
Stratix3													
StratixGX		4		4								2	
Stratix2GX				4								2	
Max2		4		4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion													
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4EB

4-Bit D Flip-Flop with Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				4									
Cyclone		4		4								1	
Cyclone2				4									
Cyclone3		4		4									
Stratix		4		4								1	
Stratix2				4									
Stratix3													
StratixGX		4		4								1	
Stratix2GX				4								1	
Max2		4		4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		4											
ProAsic3E		4											
Fusion													
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4ES

4-Bit D Flip-Flop with Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				4									
Cyclone		4		4								1	
Cyclone2				4									
Cyclone3		4		4									
Stratix		4		4								1	
Stratix2				4									
Stratix3													
StratixGX		4		4								1	
Stratix2GX				4								1	
Max2		4		4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		4											
ProAsic3E		4											
Fusion													
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4PB

4-Bit D-Type Flip-Flop with Asynchronous Preset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	4									
Cyclone		8	4	4								2	
Cyclone2		8	4	4									
Cyclone3		8	8	4									
Stratix		8	4	4								2	
Stratix2		8	4	4									
Stratix3													
StratixGX		8	4	4								2	
Stratix2GX			8	4								2	
Max2		8	4	4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion													
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4PEB

4-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	4									
Cyclone		8	4	4								2	
Cyclone2		8	4	4									
Cyclone3		8	8	4									
Stratix		8	4	4								2	
Stratix2		8	4	4									
Stratix3													
StratixGX		8	4	4								2	
Stratix2GX			8	4								2	
Max2		8	4	4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4PES

4-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	4									
Cyclone		8	4	4								2	
Cyclone2		8	4	4									
Cyclone3		8	8	4									
Stratix		8	4	4								2	
Stratix2		8	4	4									
Stratix3													
StratixGX		8	4	4								2	
Stratix2GX			8	4								2	
Max2		8	4	4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4PS

4-Bit D-Type Flip-Flop with Asynchronous Preset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	4									
Cyclone		8	4	4								2	
Cyclone2		8	4	4									
Cyclone3		8	8	4									
Stratix		8	4	4								2	
Stratix2		8	4	4									
Stratix3													
StratixGX		8	4	4								2	
Stratix2GX			8	4								2	
Max2		8	4	4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion													
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4RB

4-Bit D-Type Flip-Flop with Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4									
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		4											
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8	4	4									
XP2		8		4									

FD4REB

4-Bit D-Type Flip-Flop with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		5	5	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4									
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		8	4	4									
ECP		8	4	4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8	4										
XP		8	4	4									
XP2		8		4									

FD4RES

4-Bit D-Type Flip-Flop with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		5	5	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		8	4	4									
ECP		8	4	4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8	4										
XP		8	4	4									
XP2		8		4									

FD4RS

4-Bit D-Type Flip-Flop with Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		4											
EC		8	4	4									
ECP		8	4	4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8	4	4									
XP2		8		4									

FD4RSB

4-Bit D-Type Flip-Flop with Synchronous Reset and Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		8		4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		4											
EC		8	4	4									
ECP		8	4	4									
ECP2		8	4	4									
ECP2M		8	4	4									
SC		8	4	4									
MACHXO		8	4										
XP		8	4	4									
XP2		8	4	4									

FD4RSEB

4-Bit D-Type Flip-Flop with Synchronous Reset and Set and Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		8	8	4								1	
Cyclone2		8	8	4									
Cyclone3		5	5	4									
Stratix		8	8	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		8	8	4								1	
Stratix2GX			4	4								1	
Max2		8	8	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		8		4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		8	4	4									
ECP		8	4	4									
ECP2		10	5	4									
ECP2M		10	5	4									
SC		10	5	4									
MACHXO		8	4										
XP		8	8	4									
XP2		10	5	4									

FD4RSES

4-Bit D-Type Flip-Flop with Synchronous Reset and Set and Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	4									
Cyclone		8	8	4								1	
Cyclone2		8	8	4									
Cyclone3		5	5	4									
Stratix		8	8	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		8	8	4								1	
Stratix2GX			4	4								1	
Max2		8	8	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		8		4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		8	8	4									
ECP		8	8	4									
ECP2		10	5	4									
ECP2M		10	5	4									
SC		10	5	4									
MACHXO		8	4										
XP		8	8	4									
XP2		10	5	4									

FD4RSS

4-Bit D-Type Flip-Flop with Synchronous Reset and Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		8		4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		4											
EC		8	4	4									
ECP		8	4	4									
ECP2		8	4	4									
ECP2M		8	4	4									
SC		8	4	4									
MACHXO		8	4										
XP		8	4	4									
XP2		8	4	4									

FD4S

4-Bit D-Type Flip-Flop, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				4									
Cyclone		4		4								1	
Cyclone2				4									
Cyclone3		4		4									
Stratix		4		4								1	
Stratix2				4									
Stratix3													
StratixGX		4		4									
Stratix2GX				4								1	
Max2		4		4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion													
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8		4									
XP2		8		4									

FD4SB

4-Bit D-Type Flip-Flop with Synchronous Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		4											
EC		8		4									
ECP		8		4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8	4	4									
XP2		8		4									

FD4SEB

4-Bit D-Type Flip-Flop with Clock Enable and Synchronous Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		5	5	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4									
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4										
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		8	4	4									
ECP		8	4	4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8	4										
XP		8	4	4									
XP2		8		4									

FD4SES

4-Bit D-Type Flip-Flop with Clock Enable and Synchronous Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		5	5	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		8	4	4									
ECP		8	4	4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8	4										
XP		8	4	4									
XP2		8		4									

FD4SRB

4-Bit D-Type Flip-Flop with Synchronous Set and Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8	8	4									
Spartan2E		8	8	4									
Spartan3		8	8	4									
Spartan3A		8	8	4									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	4									
Spartan3L		8	8	4									
Virtex		8	8	4									
Virtex2		8	8	4									
Virtex2p		8	8	4									
VirtexE		8	8	4									
Virtex4		8	8	4									
Virtex5		12	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		4											
EC		8	4	4									
ECP		8	4	4									
ECP2		8	4	4									
ECP2M		8	4	4									
SC		8	4	4									
MACHXO		8	4										
XP		8	4	4									
XP2		8	4	4									

FD4SREB

4-Bit D-Type Flip-Flop with Synchronous Set and Reset and Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		8	8	4								1	
Cyclone2		8	8	4									
Cyclone3		5	5	4									
Stratix		8	8	4								1	
Stratix2		4	4	4									
Stratix3													
StratixGX		8	8	4								1	
Stratix2GX			4	4								1	
Max2		8	8	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		10	9	4									
Spartan2E		10	9	4									
Spartan3		10	9	4									
Spartan3A		10	9	4									
Spartan3ADSP		10	9										
Spartan3AN		10	9										
Spartan3E		10	9	4									
Spartan3L		10	9	4									
Virtex		10	9	4									
Virtex2		10	9	4									
Virtex2p		10	9	4									
VirtexE		10	9	4									
Virtex4		10	9	4									
Virtex5		14	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		17											
ProAsic3		17											
ProAsic3E		17											
Fusion		17											
EC		8	4	4									
ECP		8	4	4									
ECP2		10	5	4									
ECP2M		10	5	4									
SC		10	5	4									
MACHXO		8	4										
XP		10	9	4									
XP2		10	5	4									

FD4SRES

4-Bit D-Type Flip-Flop with Synchronous Set and Reset and Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		8	8	4								1	
Cyclone2		8	8	4									
Cyclone3		5	5	4									
Stratix		8	8	4								1	
Stratix2		4	4	4									
Stratix3			5	4								1	
StratixGX		8	8	4								1	
Stratix2GX			4	4								1	
Max2		8	8	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		10	9	4									
Spartan2E		10	9	4									
Spartan3		10	9	4									
Spartan3A		10	9	4									
Spartan3ADSP		10	9										
Spartan3AN		10	9										
Spartan3E		10	9	4									
Spartan3L		10	9	4									
Virtex		10	9	4									
Virtex2		10	9	4									
Virtex2p		10	9	4									
VirtexE		10	9	4									
Virtex4		10	9	4									
Virtex5		14	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		17											
ProAsic3		17											
ProAsic3E		17											
Fusion		17											
EC		8	8	4									
ECP		8	8	4									
ECP2		10	5	4									
ECP2M		10	5	4									
SC		10	5	4									
MACHXO		8	4										
XP		10	9	4									
XP2		10	5	4									

FD4SRS

4-Bit D-Type Flip-Flop with Synchronous Set and Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3			4	4								1	
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8	8	4									
Spartan2E		8	8	4									
Spartan3		8	8	4									
Spartan3A		8	8	4									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	4									
Spartan3L		8	8	4									
Virtex		8	8	4									
Virtex2		8	8	4									
Virtex2p		8	8	4									
VirtexE		8	8	4									
Virtex4		8	8	4									
Virtex5		12	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		4											
EC		8	4	4									
ECP		8	4	4									
ECP2		8	4	4									
ECP2M		8	4	4									
SC		8	4	4									
MACHXO		8	4										
XP		8	4	4									
XP2		8	4	4									

FD4SS

4-Bit D-Type Flip-Flop with Synchronous Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3			4	4								1	
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		4	4	4									
Spartan2E		4	4	4									
Spartan3		4	4	4									
Spartan3A		4	4	4									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	4									
Spartan3L		4	4	4									
Virtex		4	4	4									
Virtex2		4	4	4									
Virtex2p		4	4	4									
VirtexE		4	4	4									
Virtex4		12	4	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		4											
EC		8	4	4									
ECP		8	4	4									
ECP2		8		4									
ECP2M		8		4									
SC		8		4									
MACHXO		8											
XP		8	4	4									
XP2		8		4									

FD8B

8-Bit D-Type Flip-Flop, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								1	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8		8								1	
Stratix2				8									
Stratix3				8								1	
StratixGX		8		8								1	
Stratix2GX				8								1	
Max2		8		8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion													
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8CB

8-Bit D-Type Flip-Flop with Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								2	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8		8								2	
Stratix2				8									
Stratix3				8								2	
StratixGX		8		8								2	
Stratix2GX				8								2	
Max2		8		8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion													
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8CEB

8-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								2	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8		8								2	
Stratix2				8									
Stratix3				8								2	
StratixGX		8		8								2	
Stratix2GX				8								2	
Max2		8		8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8CES

8-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								2	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8		8								2	
Stratix2				8									
Stratix3				8								2	
StratixGX		8		8								2	
Stratix2GX				8								2	
Max2		8		8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8CPB

8-Bit D-Type Flip-Flop with Asynchronous Preset and Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								3	
Cyclone2		18		8									
Cyclone3		18	18	8									
Stratix		8		8								3	
Stratix2				8									
Stratix3			18	8								2	
StratixGX		8		8								3	
Stratix2GX				8								3	
Max2		8		8								3	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		16		8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		32											
Fusion		32											
EC		20	10	9									
ECP		20	10	9									
ECP2		32	9	16									
ECP2M		32	9	16									
SC		34	9	17									
MACHXO		20	10										
XP		20	10	9									
XP2		32	9	16									

FD8CPEB

8-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								3	
Cyclone2		26	8	8									
Cyclone3		26	26	8									
Stratix		8	8	8								3	
Stratix2		8	8	8									
Stratix3			18	8								2	
StratixGX		16	8	8									
Stratix2GX			8	8								3	
Max2		16	8	8								3	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		16		8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		40											
ProAsic3		40											
ProAsic3E		40											
Fusion		40											
EC		20	10	9									
ECP		20	10	9									
ECP2		32	17	16									
ECP2M		32	17	16									
SC		34	17	17									
MACHXO		20	10										
XP		20	10	9									
XP2		32	17	16									

FD8CPES

8-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								3	
Cyclone2		26	8	8									
Cyclone3		26	26	8									
Stratix		8	8	8								3	
Stratix2		8	8	8									
Stratix3			18	8								2	
StratixGX		8	8	8								3	
Stratix2GX			8	8								3	
Max2		16	8	8								3	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		16		8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		40											
ProAsic3		40											
ProAsic3E		40											
Fusion		40											
EC		20	10	9									
ECP		20	10	9									
ECP2		32	17	16									
ECP2M		32	17	16									
SC		34	17	17									
MACHXO		20	10										
XP		20	10	9									
XP2		32	17	16									

FD8CPS

8-Bit D-Type Flip-Flop with Asynchronous Preset and Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								3	
Cyclone2		18		8									
Cyclone3		18	18	8									
Stratix		8		8								3	
Stratix2				8									
Stratix3			18	8								2	
StratixGX		8		8								3	
Stratix2GX				8								3	
Max2		8		8								3	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		16		8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		32											
Fusion		32											
EC		20	10	9									
ECP		20	10	9									
ECP2		32	9	16									
ECP2M		32	9	16									
SC		34	9	17									
MACHXO		20	10										
XP		20	10	9									
XP2		32	9	16									

FD8CS

8-Bit D-Type Flip-Flop with Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								2	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8		8								2	
Stratix2				8									
Stratix3				8								2	
StratixGX		8		8								2	
Stratix2GX				8								2	
Max2		8		8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion													
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8EB

8-Bit D Flip-Flop with Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								1	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8		8								1	
Stratix2				8									
Stratix3				8								1	
StratixGX		8		8								1	
Stratix2GX				8								1	
Max2		8		8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		8											
ProAsic3E		8											
Fusion													
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8ES

8-Bit D Flip-Flop with Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								1	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8		8								1	
Stratix2				8									
Stratix3				8								1	
StratixGX		8		8								1	
Stratix2GX				8								1	
Max2		8		8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		8											
ProAsic3E		8											
Fusion													
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8PB

8-Bit D-Type Flip-Flop with Asynchronous Preset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16	8									
Cyclone		16	8	8								2	
Cyclone2		16	8	8									
Cyclone3		16	16	8									
Stratix		16	8	8								2	
Stratix2		16	8	8									
Stratix3			16	8								2	
StratixGX		16	8	8									
Stratix2GX			16	8								2	
Max2		16	8	8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion													
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8PEB

8-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16	8									
Cyclone		16	8	8								2	
Cyclone2		16	8	8									
Cyclone3		16	16	8									
Stratix		16	8	8								2	
Stratix2		16	8	8									
Stratix3			16	8								2	
StratixGX		16	8	8								2	
Stratix2GX			16	8								2	
Max2		16	8	8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8PES

8-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16	8									
Cyclone		16	8	8								2	
Cyclone2		16	8	8									
Cyclone3		16	16	8									
Stratix		16	8	8								2	
Stratix2		16	8	8									
Stratix3			16	8								2	
StratixGX		16	8	8								2	
Stratix2GX			16	8								2	
Max2		16	8	8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8PS

8-Bit D-Type Flip-Flop with Asynchronous Preset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16	8									
Cyclone		16	8	8								2	
Cyclone2		16	8	8									
Cyclone3		16	16	8									
Stratix		16	8	8								2	
Stratix2		16	8	8									
Stratix3			16	8								2	
StratixGX		16	8	8								2	
Stratix2GX			16	8								2	
Max2		16	8	8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion													
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8RB

8-Bit D-Type Flip-Flop with Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								1	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8		8								1	
Stratix2		8	8	8									
Stratix3				8								1	
StratixGX		8		8								1	
Stratix2GX				8								1	
Max2		8		8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L													
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		8											
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16	8	8									
XP2		16		8									

FD8REB

8-Bit D-Type Flip-Flop with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	8									
Cyclone		9	1	8								1	
Cyclone2		1	1	8									
Cyclone3		8	1	8									
Stratix		9	1	8								1	
Stratix2		8	8	8									
Stratix3			1	8								1	
StratixGX		9	1	8									
Stratix2GX			1	8								1	
Max2		9	1	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L													
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16	8										
XP		16	8	8									
XP2		16		8									

FD8RES

8-Bit D-Type Flip-Flop with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	8									
Cyclone		9	1	8								1	
Cyclone2		1	1	8									
Cyclone3		8	1	8									
Stratix		9	1	8								1	
Stratix2		8	8	8									
Stratix3			1	8								1	
StratixGX		9	1	8								1	
Stratix2GX			1	8								1	
Max2		9	1	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L													
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16	8										
XP		16	8	8									
XP2		16		8									

FD8RS

8-Bit D-Type Flip-Flop with Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								1	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8		8								1	
Stratix2		8	8	8									
Stratix3				8								1	
StratixGX		8		8								1	
Stratix2GX				8								1	
Max2		8		8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L													
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		8											
EC		16	8	8									
ECP		16	8	8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16	8	8									
XP2		16		8									

FD8RSB

8-Bit D-Type Flip-Flop with Synchronous Reset and Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								1	
Cyclone2		8	8	8									
Cyclone3		8	8	8									
Stratix		8	8	8								1	
Stratix2		8	8	8									
Stratix3			8	8								1	
StratixGX		8	8	8									
Stratix2GX			8	8								1	
Max2		8	8	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L													
Virtex		16		8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		8											
EC		16	8	8									
ECP		16	8	8									
ECP2		16	8	8									
ECP2M		16	8	8									
SC		16	8	8									
MACHXO		16	8										
XP		16	8	8									
XP2		16	8	8									

FD8RSEB

8-Bit D-Type Flip-Flop with Synchronous Reset and Set and Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9	8									
Cyclone		8	8	8								1	
Cyclone2		8	8	8									
Cyclone3		9	9	8									
Stratix		8	8	8								1	
Stratix2		8	8	8									
Stratix3			9	8								1	
StratixGX		8	8	8								1	
Stratix2GX			8	8								1	
Max2		8	8	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		16		8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		18	9	8									
ECP2M		18	9	8									
SC		18	9	8									
MACHXO		16	8										
XP		16	16	8									
XP2		18	9	8									

FD8RSES

8-Bit D-Type Flip-Flop with Synchronous Reset and Set and Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9	8									
Cyclone		8	8	8								1	
Cyclone2		8	8	8									
Cyclone3		9	9	8									
Stratix		8	8	8								1	
Stratix2		8	8	8									
Stratix3			9	8								1	
StratixGX		8	8	8								1	
Stratix2GX			8	8								1	
Max2		8	8	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		16		8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		16	16	8									
ECP		16	16	8									
ECP2		18	9	8									
ECP2M		18	9	8									
SC		18	9	8									
MACHXO		16	8										
XP		16	16	8									
XP2		18	9	8									

FD8RSS

8-Bit D-Type Flip-Flop with Synchronous Reset and Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								1	
Cyclone2		8	8	8									
Cyclone3		8	8	8									
Stratix		8	8	8								1	
Stratix2		8	8	8									
Stratix3			8	8								1	
StratixGX		8	8	8									
Stratix2GX			8	8								1	
Max2		8	8	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		16		8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		8											
EC		16	8	8									
ECP		16	8	8									
ECP2		16	8	8									
ECP2M		16	8	8									
SC		16	8	8									
MACHXO		16	8										
XP		16	8	8									
XP2		16	8	8									

FD8S

8-Bit D-Type Flip-Flop, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				8									
Cyclone		8		8								1	
Cyclone2				8									
Cyclone3		8		8									
Stratix		8		8								1	
Stratix2				8									
Stratix3				8								1	
StratixGX		8		8								1	
Stratix2GX				8								1	
Max2		8		8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion													
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16		8									
XP2		16		8									

FD8SB

8-Bit D-Type Flip-Flop with Synchronous Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								1	
Cyclone2		8	8	8									
Cyclone3		8	8	8									
Stratix		8	8	8								1	
Stratix2		8	8	8									
Stratix3			8	8								1	
StratixGX		8	8	8								1	
Stratix2GX			8	8								1	
Max2		8	8	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		8											
EC		16		8									
ECP		16		8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16	8	8									
XP2		16		8									

FD8SEB

8-Bit D-Type Flip-Flop with Clock Enable and Synchronous Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								1	
Cyclone2		8	8	8									
Cyclone3		9	9	8									
Stratix		8	8	8								1	
Stratix2		8	8	8									
Stratix3			9	8								1	
StratixGX		8	8	8								1	
Stratix2GX			8	8								1	
Max2		8	8	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8										
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16	8										
XP		16	8	8									
XP2		16		8									

FD8SES

8-Bit D-Type Flip-Flop with Clock Enable and Synchronous Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								1	
Cyclone2		8	8	8									
Cyclone3		9	9	8									
Stratix		8	8	8								1	
Stratix2		8	8	8									
Stratix3			9	8								1	
StratixGX		8	8	8								1	
Stratix2GX			8	8								1	
Max2		8	8	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16	8										
XP		16	8	8									
XP2		16		8									

FD8SRB

8-Bit D-Type Flip-Flop with Synchronous Set and Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								1	
Cyclone2		8	8	8									
Cyclone3		8	8	8									
Stratix		8	8	8								1	
Stratix2		8	8	8									
Stratix3			8	8								1	
StratixGX		8	8	8								1	
Stratix2GX			8	8								1	
Max2		8	8	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16	16	8									
Spartan2E		16	16	8									
Spartan3		16	16	8									
Spartan3A		16	16	8									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	8									
Spartan3L		16	16	8									
Virtex		16	16	8									
Virtex2		16	16	8									
Virtex2p		16	16	8									
VirtexE		16	16	8									
Virtex4		16	16	8									
Virtex5		24	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		8											
EC		16	8	8									
ECP		16	8	8									
ECP2		16	8	8									
ECP2M		16	8	8									
SC		16	8	8									
MACHXO		16	8										
XP		16	8	8									
XP2		16	8	8									

FD8SREB

8-Bit D-Type Flip-Flop with Synchronous Set and Reset and Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		16	16	8								1	
Cyclone2		16	16	8									
Cyclone3		9	9	8									
Stratix		16	16	8								1	
Stratix2		8	8	8									
Stratix3			9	8								1	
StratixGX		16	16	8								1	
Stratix2GX			8	8								1	
Max2		16	16	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		18	17	8									
Spartan2E		18	17	8									
Spartan3		18	17	8									
Spartan3A		18	17	8									
Spartan3ADSP		18	17										
Spartan3AN		18	17										
Spartan3E		18	17	8									
Spartan3L		18	17	8									
Virtex		18	17	8									
Virtex2		18	17	8									
Virtex2p		18	17	8									
VirtexE		18	17	8									
Virtex4		18	17	8									
Virtex5		26	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		33											
ProAsic3		33											
ProAsic3E		33											
Fusion		33											
EC		16	8	8									
ECP		16	8	8									
ECP2		18	9	8									
ECP2M		18	9	8									
SC		18	9	8									
MACHXO		16	8										
XP		18	17	8									
XP2		18	9	8									

FD8SRES

8-Bit D-Type Flip-Flop with Synchronous Set and Reset and Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		16	16	8								1	
Cyclone2		16	16	8									
Cyclone3		9	9	8									
Stratix		16	16	8								1	
Stratix2		8	8	8									
Stratix3			9	8								1	
StratixGX		16	16	8								1	
Stratix2GX			8	8								1	
Max2		16	16	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		18	17	8									
Spartan2E		18	17	8									
Spartan3		18	17	8									
Spartan3A		18	17	8									
Spartan3ADSP		18	17										
Spartan3AN		18	17										
Spartan3E		18	17	8									
Spartan3L		18	17	8									
Virtex		18	17	8									
Virtex2		18	17	8									
Virtex2p		18	17	8									
VirtexE		18	17	8									
Virtex4		18	17	8									
Virtex5		22	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		33											
ProAsic3		33											
ProAsic3E		33											
Fusion		33											
EC		16	16	8									
ECP		16	16	8									
ECP2		18	9	8									
ECP2M		18	9	8									
SC		18	9	8									
MACHXO		16	8										
XP		18	17	8									
XP2		18	9	8									

FD8SRS

8-Bit D-Type Flip-Flop with Synchronous Set and Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								1	
Cyclone2		8	8	8									
Cyclone3		8	8	8									
Stratix		8	8	8								1	
Stratix2		8	8	8									
Stratix3			8	8								1	
StratixGX		8	8	8								1	
Stratix2GX			8	8								1	
Max2		8	8	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16	16	8									
Spartan2E		16	16	8									
Spartan3		16	16	8									
Spartan3A		16	16	8									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	8									
Spartan3L		16	16	8									
Virtex		16	16	8									
Virtex2		16	16	8									
Virtex2p		16	16	8									
VirtexE		16	16	8									
Virtex4		16	16	8									
Virtex5		18	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		8											
EC		16	8	8									
ECP		16	8	8									
ECP2		16	8	8									
ECP2M		16	8	8									
SC		16	8	8									
MACHXO		16	8										
XP		16	8	8									
XP2		16	8	8									

FD8SS

8-Bit D-Type Flip-Flop with Synchronous Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								1	
Cyclone2		8	8	8									
Cyclone3		8	8	8									
Stratix		8	8	8								1	
Stratix2		8	8	8									
Stratix3			8	8								1	
StratixGX		8	8	8								1	
Stratix2GX			8	8								1	
Max2		8	8	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8	8	8									
Spartan2E		8	8	8									
Spartan3		8	8	8									
Spartan3A		8	8	8									
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8	8									
Spartan3L		8	8	8									
Virtex		8	8	8									
Virtex2		8	8	8									
Virtex2p		8	8	8									
VirtexE		8	8	8									
Virtex4		24	8	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		16											
Fusion		8											
EC		16	8	8									
ECP		16	8	8									
ECP2		16		8									
ECP2M		16		8									
SC		16		8									
MACHXO		16											
XP		16	8	8									
XP2		16		8									

FD16B

16-Bit D-Type Flip-Flop, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								1	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16		16								1	
Stratix2				16									
Stratix3				16								1	
StratixGX		16		16								1	
Stratix2GX				16								1	
Max2		16		16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		17											
Fusion													
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16CB

16-Bit D-Type Flip-Flop with Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								2	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16		16								2	
Stratix2				16									
Stratix3				16								2	
StratixGX		16		16								2	
Stratix2GX				16								2	
Max2		16		16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		18											
Fusion													
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16CEB

16-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								2	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16		16								2	
Stratix2				16									
Stratix3				16								2	
StratixGX		16		16								2	
Stratix2GX				16								2	
Max2		16		16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		35											
Fusion		32											
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16CES

16-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								2	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16		16								2	
Stratix2				16									
Stratix3				16								2	
StratixGX		16		16								2	
Stratix2GX				16								2	
Max2		16		16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		35											
Fusion		32											
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16CPB

16-Bit D-Type Flip-Flop with Asynchronous Preset and Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								3	
Cyclone2		34		16									
Cyclone3		34	34	16									
Stratix		16		16								3	
Stratix2				16									
Stratix3			34	16								2	
StratixGX		16		16								3	
Stratix2GX				16								3	
Max2		16		16								3	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		32		16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		64											
ProAsic3		64											
ProAsic3E		67											
Fusion		64											
EC		36	18	17									
ECP		36	18	17									
ECP2		64	17	32									
ECP2M		64	17	32									
SC		66	17	33									
MACHXO		36	18										
XP		36	18	17									
XP2		64	17	32									

FD16CPEB

16-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16	16									
Cyclone		16	16	16								3	
Cyclone2		50	16	16									
Cyclone3		50	50	16									
Stratix		16	16	16								3	
Stratix2		16	16	16									
Stratix3			34	16								2	
StratixGX		16	16	16								3	
Stratix2GX			16	16								3	
Max2		32	16	16								3	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		32		16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		80											
ProAsic3		80											
ProAsic3E		84											
Fusion		80											
EC		36	18	17									
ECP		36	18	17									
ECP2		64	33	32									
ECP2M		64	33	32									
SC		66	33	33									
MACHXO		36	18										
XP		36	18	17									
XP2		64	33	32									

FD16CPES

16-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16	16									
Cyclone		16	16	16								3	
Cyclone2		50	16	16									
Cyclone3		50	50	16									
Stratix		16	16	16								3	
Stratix2		16	16	16									
Stratix3			34	16								2	
StratixGX		16	16	16								3	
Stratix2GX			16	16								3	
Max2		32	16	16								3	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		32		16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		80											
ProAsic3		80											
ProAsic3E		84											
Fusion		80											
EC		36	18	17									
ECP		36	18	17									
ECP2		64	33	32									
ECP2M		64	33	32									
SC		66	33	33									
MACHXO		36	18										
XP		36	18	17									
XP2		64	33	32									

FD16CPS

16-Bit D-Type Flip-Flop with Asynchronous Preset and Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								3	
Cyclone2		34		16									
Cyclone3		34	34	16									
Stratix		16		16								3	
Stratix2				16									
Stratix3			34	16								2	
StratixGX		16		16								3	
Stratix2GX				16								3	
Max2		16		16								3	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		32		16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		64											
ProAsic3		64											
ProAsic3E		67											
Fusion		64											
EC		36	18	17									
ECP		36	18	17									
ECP2		64	17	32									
ECP2M		64	17	32									
SC		66	17	33									
MACHXO		36	18										
XP		36	18	17									
XP2		64	17	32									

FD16CS

16-Bit D-Type Flip-Flop with Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								2	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16		16								2	
Stratix2				16									
Stratix3				16								2	
StratixGX		16		16									
Stratix2GX				16								2	
Max2		16		16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A													
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		18											
Fusion													
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16EB

16-Bit D Flip-Flop with Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								1	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16		16								1	
Stratix2				16									
Stratix3				16								1	
StratixGX		16		16								1	
Stratix2GX				16								1	
Max2		16		16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		16											
ProAsic3E		18											
Fusion													
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16ES

16-Bit D Flip-Flop with Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								1	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16		16								1	
Stratix2				16									
Stratix3				16								1	
StratixGX		16		16									
Stratix2GX				16								1	
Max2		16		16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		16											
ProAsic3E		18											
Fusion													
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16PB

16-Bit D-Type Flip-Flop with Asynchronous Preset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32	16									
Cyclone		32	16	16								2	
Cyclone2		32	16	16									
Cyclone3		32	32	16									
Stratix		32	16	16								2	
Stratix2		32	16	16									
Stratix3			32	16								2	
StratixGX		32	16	16								2	
Stratix2GX			32	16								2	
Max2		32	16	16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		18											
Fusion													
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16PEB

16-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32	16									
Cyclone		32	16	16								2	
Cyclone2		32	16	16									
Cyclone3		32	32	16									
Stratix		32	16	16								2	
Stratix2		32	16	16									
Stratix3			32	16								2	
StratixGX		32	16	16								2	
Stratix2GX			32	16								2	
Max2		32	16	16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		35											
Fusion		32											
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16PES

16-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32	16									
Cyclone		32	16	16								2	
Cyclone2		32	16	16									
Cyclone3		32	32	16									
Stratix		32	16	16								2	
Stratix2		32	16	16									
Stratix3			32	16								2	
StratixGX		32	16	16								2	
Stratix2GX			32	16								2	
Max2		32	16	16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		35											
Fusion		32											
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16PS

16-Bit D-Type Flip-Flop with Asynchronous Preset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32	16									
Cyclone		32	16	16								2	
Cyclone2		32	16	16									
Cyclone3		32	32	16									
Stratix		32	16	16								2	
Stratix2		32	16	16									
Stratix3			32	16								2	
StratixGX		32	16	16								2	
Stratix2GX			32	16								2	
Max2		32	16	16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		18											
Fusion													
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16RB

16-Bit D-Type Flip-Flop with Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								1	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16		16								1	
Stratix2				16									
Stratix3				16								1	
StratixGX		16		16								1	
Stratix2GX				16								1	
Max2		16		16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		34											
Fusion		16											
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32	16	16									
XP2		32		16									

FD16REB

16-Bit D-Type Flip-Flop with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		17	1	16								1	
Cyclone2		1	1	16									
Cyclone3		16	1	16									
Stratix		17	1	16								1	
Stratix2		1	1	16									
Stratix3			1	16								1	
StratixGX		17	1	16								1	
Stratix2GX			1	16								1	
Max2		17	1	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		48											
ProAsic3		48											
ProAsic3E		51											
Fusion		48											
EC		32	16	16									
ECP		32	16	16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32	16										
XP		32	16	16									
XP2		32		16									

FD16RES

16-Bit D-Type Flip-Flop with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		17	1	16								1	
Cyclone2		1	1	16									
Cyclone3		16	1	16									
Stratix		17	1	16								1	
Stratix2		1	1	16									
Stratix3			1	16								1	
StratixGX		17	1	16								1	
Stratix2GX			1	16								1	
Max2		17	1	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		48											
ProAsic3		48											
ProAsic3E		51											
Fusion		48											
EC		32	16	16									
ECP		32	16	16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32	16										
XP		32	16	16									
XP2		32		16									

FD16RS

16-Bit D-Type Flip-Flop with Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								1	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16		16								1	
Stratix2				16									
Stratix3				16								1	
StratixGX		16		16									
Stratix2GX				16								1	
Max2		16		16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		34											
Fusion		16											
EC		32	16	16									
ECP		32	16	16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32	16	16									
XP2		32		16									

FD16RSB

16-Bit D-Type Flip-Flop with Synchronous Reset and Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16	16									
Cyclone		16	16	16								1	
Cyclone2		16	16	16									
Cyclone3		16	16	16									
Stratix		16	16	16								1	
Stratix2		16	16	16									
Stratix3			16	16								1	
StratixGX		16	16	16								1	
Stratix2GX			16	16								1	
Max2		16	16	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		32		16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		35											
Fusion		16											
EC		32	16	16									
ECP		32	16	16									
ECP2		32	16	16									
ECP2M		32	16	16									
SC		32	16	16									
MACHXO		32	16										
XP		32	16	16									
XP2		32	16	16									

FD16RSEB

16-Bit D-Type Flip-Flop with Synchronous Reset and Set and Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17	16									
Cyclone		16	16	16								1	
Cyclone2		32	32	16									
Cyclone3		17	17	16									
Stratix		16	16	16								1	
Stratix2		16	16	16									
Stratix3			17	16								1	
StratixGX		16	16	16								1	
Stratix2GX			16	16								1	
Max2		32	32	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		32		16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		48											
ProAsic3		48											
ProAsic3E		52											
Fusion		48											
EC		32	16	16									
ECP		32	16	16									
ECP2		34	17	16									
ECP2M		34	17	16									
SC		34	17	16									
MACHXO		32	16										
XP		32	32	16									
XP2		34	17	16									

FD16RSES

16-Bit D-Type Flip-Flop with Synchronous Reset and Set and Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17	16									
Cyclone		16	16	16								1	
Cyclone2		32	32	16									
Cyclone3		17	17	16									
Stratix		16	16	16								1	
Stratix2		16	16	16									
Stratix3			17	16								1	
StratixGX		16	16	16									
Stratix2GX			16	16								1	
Max2		32	32	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		32		16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		48											
ProAsic3		48											
ProAsic3E		52											
Fusion		48											
EC		32	32	16									
ECP		32	32	16									
ECP2		34	17	16									
ECP2M		34	17	16									
SC		34	17	16									
MACHXO		32	16										
XP		32	32	16									
XP2		34	17	16									

FD16RSS

16-Bit D-Type Flip-Flop with Synchronous Reset and Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16	16									
Cyclone		16	16	16								1	
Cyclone2		16	16	16									
Cyclone3		16	16	16									
Stratix		16	16	16								1	
Stratix2		16	16	16									
Stratix3			16	16								1	
StratixGX		16	16	16								1	
Stratix2GX			16	16								1	
Max2		16	16	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		32		16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		35											
Fusion		16											
EC		32	16	16									
ECP		32	16	16									
ECP2		32	16	16									
ECP2M		32	16	16									
SC		32	16	16									
MACHXO		32	16										
XP		32	16	16									
XP2		32	16	16									

FD16S

16-Bit D-Type Flip-Flop, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16		16								1	
Cyclone2				16									
Cyclone3		16		16									
Stratix		16		16								1	
Stratix2				16									
Stratix3				16								1	
StratixGX		16		16									
Stratix2GX				16								1	
Max2		16		16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		16											
ProAsic3		16											
ProAsic3E		17											
Fusion													
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32		16									
XP2		32		16									

FD16SB

16-Bit D-Type Flip-Flop with Synchronous Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16	16	16								1	
Cyclone2		16	16	16									
Cyclone3		16		16									
Stratix		16	16	16								1	
Stratix2		16	16	16									
Stratix3				16								1	
StratixGX		16	16	16									
Stratix2GX				16								1	
Max2		16	16	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		34											
Fusion		16											
EC		32		16									
ECP		32		16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32	16	16									
XP2		32		16									

FD16SEB

16-Bit D-Type Flip-Flop with Clock Enable and Synchronous Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		16	16	16								1	
Cyclone2		16	16	16									
Cyclone3		16	1	16									
Stratix		16	16	16								1	
Stratix2		16	16	16									
Stratix3			1	16								1	
StratixGX		16	16	16								1	
Stratix2GX			1	16								1	
Max2		16	16	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16										
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		48											
ProAsic3		48											
ProAsic3E		51											
Fusion		48											
EC		32	16	16									
ECP		32	16	16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32	16										
XP		32	16	16									
XP2		32		16									

FD16SES

16-Bit D-Type Flip-Flop with Clock Enable and Synchronous Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		16	16	16								1	
Cyclone2		16	16	16									
Cyclone3		16	1	16									
Stratix		16	16	16								1	
Stratix2		16	16	16									
Stratix3			1	16								1	
StratixGX		16	16	16								1	
Stratix2GX			1	16								1	
Max2		16	16	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		48											
ProAsic3		48											
ProAsic3E		51											
Fusion		48											
EC		32	16	16									
ECP		32	16	16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32	16										
XP		32	16	16									
XP2		32		16									

FD16SRB

16-Bit D-Type Flip-Flop with Synchronous Set and Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16	16									
Cyclone		16	16	16								1	
Cyclone2		16	16	16									
Cyclone3		16	16	16									
Stratix		16	16	16								1	
Stratix2		16	16	16									
Stratix3			16	16								1	
StratixGX		16	16	16									
Stratix2GX			16	16								1	
Max2		16	16	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32	32	16									
Spartan2E		32	32	16									
Spartan3		32	32	16									
Spartan3A		32	32	16									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	16									
Spartan3L		32	32	16									
Virtex		32	32	16									
Virtex2		32	32	16									
Virtex2p		32	32	16									
VirtexE		32	32	16									
Virtex4		32	32	16									
Virtex5		38	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		35											
Fusion		16											
EC		32	16	16									
ECP		32	16	16									
ECP2		32	16	16									
ECP2M		32	16	16									
SC		32	16	16									
MACHXO		32	16										
XP		32	16	16									
XP2		32	16	16									

FD16SREB

16-Bit D-Type Flip-Flop with Synchronous Set and Reset and Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17	16									
Cyclone		32	32	16								1	
Cyclone2		32	32	16									
Cyclone3		17	17	16									
Stratix		32	32	16								1	
Stratix2		16	16	16									
Stratix3			17	16								1	
StratixGX		32	32	16								1	
Stratix2GX			17	16								1	
Max2		32	32	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		34	33	16									
Spartan2E		34	33	16									
Spartan3		34	33	16									
Spartan3A		34	33	16									
Spartan3ADSP		34	33										
Spartan3AN		34	33										
Spartan3E		34	33	16									
Spartan3L		34	33	16									
Virtex		34	33	16									
Virtex2		34	33	16									
Virtex2p		34	33	16									
VirtexE		34	33	16									
Virtex4		34	33	16									
Virtex5		44	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		65											
ProAsic3		66											
ProAsic3E		69											
Fusion		66											
EC		32	16	16									
ECP		32	16	16									
ECP2		34	17	16									
ECP2M		34	17	16									
SC		34	17	16									
MACHXO		32	16										
XP		34	33	16									
XP2		34	17	16									

FD16SRES

16-Bit D-Type Flip-Flop with Synchronous Set and Reset and Clock Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17	16									
Cyclone		32	32	16								1	
Cyclone2		32	32	16									
Cyclone3		17	17	16									
Stratix		32	32	16								1	
Stratix2		16	16	16									
Stratix3			17	16								1	
StratixGX		32	32	16									
Stratix2GX			17	16								1	
Max2		32	32	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		34	33	16									
Spartan2E		34	33	16									
Spartan3		34	33	16									
Spartan3A		34	33	16									
Spartan3ADSP		34	33										
Spartan3AN		34	33										
Spartan3E		34	33	16									
Spartan3L		34	33	16									
Virtex		34	33	16									
Virtex2		34	33	16									
Virtex2p		34	33	16									
VirtexE		34	33	16									
Virtex4		34	33	16									
Virtex5		42	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		65											
ProAsic3		66											
ProAsic3E		69											
Fusion		66											
EC		32	32	16									
ECP		32	32	16									
ECP2		34	17	16									
ECP2M		34	17	16									
SC		34	17	16									
MACHXO		32	16										
XP		34	33	16									
XP2		34	17	16									

FD16SRS

16-Bit D-Type Flip-Flop with Synchronous Set and Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16	16									
Cyclone		16	16	16								1	
Cyclone2		16	16	16									
Cyclone3		16	16	16									
Stratix		16	16	16								1	
Stratix2		16	16	16									
Stratix3			16	16								1	
StratixGX		16	16	16								1	
Stratix2GX			16	16								1	
Max2		16	16	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32	32	16									
Spartan2E		32	32	16									
Spartan3		32	32	16									
Spartan3A		32	32	16									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	16									
Spartan3L		32	32	16									
Virtex		32	32	16									
Virtex2		32	32	16									
Virtex2p		32	32	16									
VirtexE		32	32	16									
Virtex4		32	32	16									
Virtex5		48	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		35											
Fusion		16											
EC		32	16	16									
ECP		32	16	16									
ECP2		32	16	16									
ECP2M		32	16	16									
SC		32	16	16									
MACHXO		32	16										
XP		32	16	16									
XP2		32	16	16									

FD16SS

16-Bit D-Type Flip-Flop with Synchronous Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				16									
Cyclone		16	16	16								1	
Cyclone2		16	16	16									
Cyclone3		16	16	16									
Stratix		16	16	16								1	
Stratix2		16	16	16									
Stratix3				16								1	
StratixGX		16	16	16									
Stratix2GX				16								1	
Max2		16	16	16								1	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16	16	16									
Spartan2E		16	16	16									
Spartan3		16	16	16									
Spartan3A		16	16	16									
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16	16									
Spartan3L		16	16	16									
Virtex		16	16	16									
Virtex2		16	16	16									
Virtex2p		16	16	16									
VirtexE		16	16	16									
Virtex4		48	16	16									
Virtex5		16	16	10									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		32											
ProAsic3E		34											
Fusion		16											
EC		32	16	16									
ECP		32	16	16									
ECP2		32		16									
ECP2M		32		16									
SC		32		16									
MACHXO		32											
XP		32	16	16									
XP2		32		16									

FD32B

32-Bit D-Type Flip-Flop, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				32									
Cyclone		32		32								1	
Cyclone2				32									
Cyclone3		32		32									
Stratix		32		32								1	
Stratix2				32									
Stratix3													
StratixGX		32		32								1	
Stratix2GX				32								1	
Max2		32		32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		32											
ProAsic3		34											
ProAsic3E		34											
Fusion													
EC		64		32									
ECP		64		32									
ECP2		64		32									
ECP2M		64		32									
SC		64		32									
MACHXO		64											
XP		64		32									
XP2		64		32									

FD32CB

32-Bit D-Type Flip-Flop with Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				32									
Cyclone		32		32								2	
Cyclone2				32									
Cyclone3		32		32									
Stratix		32		32								2	
Stratix2				32									
Stratix3													
StratixGX		32		32								2	
Stratix2GX				32								2	
Max2		32		32								2	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		32											
ProAsic3		36											
ProAsic3E		36											
Fusion													
EC		64		32									
ECP		64		32									
ECP2		64		32									
ECP2M		64		32									
SC		64		32									
MACHXO		64											
XP		64		32									
XP2		64		32									

FD32CEB

32-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				32									
Cyclone		32		32								2	
Cyclone2				32									
Cyclone3		32		32									
Stratix		32		32								2	
Stratix2				32									
Stratix3													
StratixGX		32		32								2	
Stratix2GX				32								2	
Max2		32		32								2	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		64											
ProAsic3		70											
ProAsic3E		70											
Fusion		64											
EC		64		32									
ECP		64		32									
ECP2		64		32									
ECP2M		64		32									
SC		64		32									
MACHXO		64											
XP		64		32									
XP2		64		32									

FD32CPB

32-Bit D-Type Flip-Flop with Asynchronous Preset and Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				32									
Cyclone		32		32								3	
Cyclone2		66		32									
Cyclone3		66	66	32									
Stratix		32		32								3	
Stratix2				32									
Stratix3													
StratixGX		32		32								3	
Stratix2GX				32								3	
Max2		32		32								3	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		64		32									
Spartan2E		64		32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		64		32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		64		32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		128											
ProAsic3		134											
ProAsic3E		134											
Fusion		128											
EC		68	34	33									
ECP		68	34	33									
ECP2		128	33	64									
ECP2M		128	33	64									
SC		130	33	65									
MACHXO		68	34										
XP		68	34	33									
XP2		128	33	64									

FD32CPEB

32-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32	32									
Cyclone		32	32	32								3	
Cyclone2		98	32	32									
Cyclone3		98	98	32									
Stratix		32	32	32								3	
Stratix2		32	32	32									
Stratix3													
StratixGX		32	32	32								3	
Stratix2GX			32	32								3	
Max2		64	32	32								3	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		64		32									
Spartan2E		64		32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		64		32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		64		32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		160											
ProAsic3		168											
ProAsic3E		168											
Fusion		160											
EC		68	34	33									
ECP		68	34	33									
ECP2		128	65	64									
ECP2M		128	65	64									
SC		130	65	65									
MACHXO		68	34										
XP		68	34	33									
XP2		128	65	64									

FD32EB

32-Bit D Flip-Flop with Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				32									
Cyclone		32		32								1	
Cyclone2				32									
Cyclone3		32		32									
Stratix		32		32								1	
Stratix2				32									
Stratix3													
StratixGX		32		32								1	
Stratix2GX				32								1	
Max2		32		32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		64											
ProAsic3		36											
ProAsic3E		36											
Fusion													
EC		64		32									
ECP		64		32									
ECP2		64		32									
ECP2M		64		32									
SC		64		32									
MACHXO		64											
XP		64		32									
XP2		64		32									

FD32PB

32-Bit D-Type Flip-Flop with Asynchronous Preset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			64	32									
Cyclone		64	32	32								2	
Cyclone2		64	32	32									
Cyclone3		64	64	32									
Stratix		64	32	32								2	
Stratix2		64	32	32									
Stratix3													
StratixGX		64	32	32								2	
Stratix2GX			64	32								2	
Max2		64	32	32								2	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		32											
ProAsic3		36											
ProAsic3E		36											
Fusion													
EC		64		32									
ECP		64		32									
ECP2		64		32									
ECP2M		64		32									
SC		64		32									
MACHXO		64											
XP		64		32									
XP2		64		32									

FD32PEB

32-Bit D-Type Flip-Flop with Clock Enable and Asynchronous Preset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			64	32									
Cyclone		64	32	32								2	
Cyclone2		64	32	32									
Cyclone3		64	64	32									
Stratix		64	32	32								2	
Stratix2		64	32	32									
Stratix3													
StratixGX		64	32	32								2	
Stratix2GX			64	32								2	
Max2		64	32	32								2	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		64											
ProAsic3		70											
ProAsic3E		70											
Fusion		64											
EC		64		32									
ECP		64		32									
ECP2		64		32									
ECP2M		64		32									
SC		64		32									
MACHXO		64											
XP		64		32									
XP2		64		32									

FD32RB

32-Bit D-Type Flip-Flop with Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				32									
Cyclone		32		32								1	
Cyclone2				32									
Cyclone3		32		32									
Stratix		32		32								1	
Stratix2				32									
Stratix3													
StratixGX		32		32								1	
Stratix2GX				32								1	
Max2		32		32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		64											
ProAsic3		68											
ProAsic3E		68											
Fusion		32											
EC		64		32									
ECP		64		32									
ECP2		64		32									
ECP2M		64		32									
SC		64		32									
MACHXO		64											
XP		64	32	32									
XP2		64		32									

FD32REB

32-Bit D-Type Flip-Flop with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	32									
Cyclone		33	1	32								1	
Cyclone2		2	2	32									
Cyclone3		32	1	32									
Stratix		33	1	32								1	
Stratix2		1	1	32									
Stratix3													
StratixGX		33	1	32								1	
Stratix2GX			2	32								1	
Max2		33	1	32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		96											
ProAsic3		102											
ProAsic3E		102											
Fusion		96											
EC		64	32	32									
ECP		64	32	32									
ECP2		64		32									
ECP2M		64		32									
SC		64		32									
MACHXO		64	32										
XP		64	32	32									
XP2		64		32									

FD32RSB

32-Bit D-Type Flip-Flop with Synchronous Reset and Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32	32									
Cyclone		32	32	32								1	
Cyclone2		32	32	32									
Cyclone3		32	32	32									
Stratix		32	32	32								1	
Stratix2		32	32	32									
Stratix3													
StratixGX		32	32	32								1	
Stratix2GX			32	32								1	
Max2		32	32	32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		64		32									
Spartan2E		64		32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		64		32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		64		32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		64											
ProAsic3		70											
ProAsic3E		70											
Fusion		32											
EC		64	32	32									
ECP		64	32	32									
ECP2		64	32	32									
ECP2M		64	32	32									
SC		64	32	32									
MACHXO		64	32										
XP		64	32	32									
XP2		64	32	32									

FD32RSEB

32-Bit D-Type Flip-Flop with Synchronous Reset and Set and Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			33	32									
Cyclone		45	45	32								1	
Cyclone2		56	56	32									
Cyclone3		33	33	32									
Stratix		45	45	32								1	
Stratix2		32	32	32									
Stratix3													
StratixGX		45	45	32								1	
Stratix2GX			32	32								1	
Max2		44	44	32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		64		32									
Spartan2E		64		32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		64		32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		64		32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		96											
ProAsic3		104											
ProAsic3E		104											
Fusion		96											
EC		64	32	32									
ECP		64	32	32									
ECP2		66	33	32									
ECP2M		66	33	32									
SC		66	33	32									
MACHXO		64	32										
XP		64	64	32									
XP2		66	33	32									

FD32SB

32-Bit D-Type Flip-Flop with Synchronous Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				32									
Cyclone		32	32	32								1	
Cyclone2		32	32	32									
Cyclone3		32		32									
Stratix		32	32	32								1	
Stratix2		32	32	32									
Stratix3													
StratixGX		32	32	32								1	
Stratix2GX				32								1	
Max2		32	32	32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		64											
ProAsic3		68											
ProAsic3E		68											
Fusion		32											
EC		64		32									
ECP		64		32									
ECP2		64		32									
ECP2M		64		32									
SC		64		32									
MACHXO		64											
XP		64	32	32									
XP2		64		32									

FD32SEB

32-Bit D-Type Flip-Flop with Clock Enable and Synchronous Set, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	32									
Cyclone		32	32	32								1	
Cyclone2		32	32	32									
Cyclone3		32	1	32									
Stratix		32	32	32								1	
Stratix2		32	32	32									
Stratix3													
StratixGX		32	32	32								1	
Stratix2GX			2	32								1	
Max2		32	32	32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32	32	32									
Spartan2E		32	32	32									
Spartan3		32	32	32									
Spartan3A		32	32	32									
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32	32									
Spartan3L		32	32	32									
Virtex		32	32	32									
Virtex2		32	32	32									
Virtex2p		32	32	32									
VirtexE		32	32	32									
Virtex4		96	32	32									
Virtex5		32	32	2									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		96											
ProAsic3		102											
ProAsic3E		102											
Fusion		96											
EC		64	32	32									
ECP		64	32	32									
ECP2		64		32									
ECP2M		64		32									
SC		64		32									
MACHXO		64	32										
XP		64	32	32									
XP2		64		32									

FD32SRB

32-Bit D-Type Flip-Flop with Synchronous Set and Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32	32									
Cyclone		32	32	32								1	
Cyclone2		32	32	32									
Cyclone3		32	32	32									
Stratix		32	32	32								1	
Stratix2		32	32	32									
Stratix3													
StratixGX		32	32	32								1	
Stratix2GX			32	32								1	
Max2		32	32	32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		64	64	32									
Spartan2E		64	64	32									
Spartan3		64	64	32									
Spartan3A		64	64	32									
Spartan3ADSP		64	64										
Spartan3AN		64	64										
Spartan3E		64	64	32									
Spartan3L		64	64	32									
Virtex		64	64	32									
Virtex2		64	64	32									
Virtex2p		64	64	32									
VirtexE		64	64	32									
Virtex4		64	64	32									
Virtex5		86	32	32									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		64											
ProAsic3		70											
ProAsic3E		70											
Fusion		32											
EC		64	32	32									
ECP		64	32	32									
ECP2		64	32	32									
ECP2M		64	32	32									
SC		64	32	32									
MACHXO		64	32										
XP		64	32	32									
XP2		64	32	32									

FD32SREB

32-Bit D-Type Flip-Flop with Synchronous Set and Reset and Clock Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			33	32									
Cyclone		65	65	32								1	
Cyclone2		64	64	32									
Cyclone3		33	33	32									
Stratix		65	65	32								1	
Stratix2		32	32	32									
Stratix3													
StratixGX		65	65	32								1	
Stratix2GX			34	32								1	
Max2		64	64	32								1	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		66	65	32									
Spartan2E		66	65	32									
Spartan3		66	65	32									
Spartan3A		66	65	32									
Spartan3ADSP		66	65										
Spartan3AN		66	65										
Spartan3E		66	65	32									
Spartan3L		66	65	32									
Virtex		66	65	32									
Virtex2		66	65	32									
Virtex2p		66	65	32									
VirtexE		66	65	32									
Virtex4		66	65	32									
Virtex5		86	32	32									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		130											
ProAsic3		136											
ProAsic3E		139											
Fusion		131											
EC		64	32	32									
ECP		64	32	32									
ECP2		66	33	32									
ECP2M		66	33	32									
SC		66	33	32									
MACHXO		64	32										
XP		66	65	32									
XP2		66	33	32									

FD_1

D-Type Negative Edge Flip-Flop

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				1									
Cyclone		1		1									
Cyclone2				1									
Cyclone3		1		1									
Stratix		1		1									
Stratix2				1									
Stratix3				1									
StratixGX		1		1									
Stratix2GX				1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion													
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDC

D-Type Flip-Flop with Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				1									
Cyclone		1		1									
Cyclone2				1									
Cyclone3		1		1									
Stratix		1		1									
Stratix2				1									
Stratix3				1									
StratixGX		1		1									
Stratix2GX				1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion													
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDC_1

D-Type Negative Edge Flip-Flop with Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				1									
Cyclone		1		1									
Cyclone2				1									
Cyclone3		1		1									
Stratix		1		1									
Stratix2				1									
Stratix3				1									
StratixGX		1		1									
Stratix2GX				1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion													
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDCE

D-Type Flip-Flop with Clock Enable and Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				1									
Cyclone		1		1									
Cyclone2				1									
Cyclone3		1		1									
Stratix		1		1									
Stratix2				1									
Stratix3				1									
StratixGX		1		1									
Stratix2GX				1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDCE_1

D-Type Negative Edge Flip-Flop with Clock Enable, Asynchronous Clear and Dual output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				1									
Cyclone		1		1									
Cyclone2				1									
Cyclone3		1		1									
Stratix		1		1									
Stratix2				1									
Stratix3				1									
StratixGX		1		1									
Stratix2GX				1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDCEN

D-Type Flip-Flop with Clock Enable, Asynchronous Clear and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L													
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FDCN

D-Type Flip-Flop with Asynchronous Clear and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L													
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FDCP

D-Type Flip-Flop with Asynchronous Preset and Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				1									
Cyclone		1		1									
Cyclone2		4		1									
Cyclone3		4	4	1									
Stratix		1		1									
Stratix2				1									
Stratix3			4	1									
StratixGX		1		1									
Stratix2GX				1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		6	3	2									
ECP		6	3	2									
ECP2		4	2	2									
ECP2M		4	2	2									
SC		6	2	3									
MACHXO		6	3										
XP		6	3	2									
XP2		4	2	2									

FDCP_1

D-Type Negative Edge Flip-Flop with Asynchronous Preset and Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				1									
Cyclone		1		1									
Cyclone2		5	1	1									
Cyclone3		5	5	1									
Stratix		1		1									
Stratix2				1									
Stratix3			4	1									
StratixGX		1		1									
Stratix2GX				1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		6	3	2									
ECP		6	3	2									
ECP2		4	2	2									
ECP2M		4	2	2									
SC		6	2	3									
MACHXO		6	3										
XP		6	3	2									
XP2		4	2	2									

FDCPE

D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		5	1	1									
Cyclone3		5	5	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			4	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		6	3	2									
ECP		6	3	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		6	3										
XP		6	3	2									
XP2		4	3	2									

FDCPE_1

D-Type Negative Edge Flip-Flop with Clock Enable and Asynchronous Preset and Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			4	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		6	3	2									
ECP		6	3	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		6	3										
XP		6	3	2									
XP2		4	3	2									

FDCPEN

D-Type Flip-Flop with Clock Enable, Asynchronous Preset, Clear and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			5	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		3	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L													
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		5											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		8	4	2									
ECP		8	4	2									
ECP2		4	4	2									
ECP2M		4	4	2									
SC		6	4	3									
MACHXO		8	4										
XP		8	4	2									
XP2		4	4	2									

FDCPN

D-Type Flip-Flop with Asynchronous Preset, Clear and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	1	1									
Cyclone2		5	1	1									
Cyclone3		5	5	1									
Stratix		2	1	1									
Stratix2		1	1	1									
Stratix3			5	1									
StratixGX		2	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		8	4	2									
ECP		8	4	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		8	4										
XP		8	4	2									
XP2		4	3	2									

FDE

D Flip-Flop with Clock Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				1									
Cyclone		1		1									
Cyclone2				1									
Cyclone3		1		1									
Stratix		1		1									
Stratix2				1									
Stratix3				1									
StratixGX		1		1									
Stratix2GX				1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion													
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDE_1

D Negative Edge Flip-Flop with Clock Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx				1									
Cyclone		1		1									
Cyclone2				1									
Cyclone3		1		1									
Stratix		1		1									
Stratix2				1									
Stratix3				1									
StratixGX		1		1									
Stratix2GX				1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		1											
ProAsic3E		1											
Fusion													
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDEN

D Flip-Flop with Clock Enable and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FDN

D-Type Flip-Flop with Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FDP

D-Type Flip-Flop with Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	1	1									
Cyclone2		2	1	1									
Cyclone3		2	2	1									
Stratix		2	1	1									
Stratix2		2	1	1									
Stratix3			2	1									
StratixGX		2	1	1									
Stratix2GX			2	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion													
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDP_1

D-Type Negative Edge Flip-Flop with Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	1	1									
Cyclone2		2	1	1									
Cyclone3		2	2	1									
Stratix		2	1	1									
Stratix2		2	1	1									
Stratix3			2	1									
StratixGX		2	1	1									
Stratix2GX			2	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		1											
ProAsic3		1											
ProAsic3E		1											
Fusion													
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDPE

D-Type Flip-Flop with Clock Enable and Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	1	1									
Cyclone2		2	1	1									
Cyclone3		2	2	1									
Stratix		2	1	1									
Stratix2		2	1	1									
Stratix3			2	1									
StratixGX		2	1	1									
Stratix2GX			2	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDPE_1

D-Type Flip-Flop with Clock Enable and Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	1	1									
Cyclone2		2	1	1									
Cyclone3		2	2	1									
Stratix		2	1	1									
Stratix2		2	1	1									
Stratix3			2	1									
StratixGX		2	1	1									
Stratix2GX			2	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2		1									
ECP		2		1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2											
XP		2		1									
XP2		2		1									

FDPEN

D-Type Flip-Flop with Clock Enable and Asynchronous Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	1	1									
Cyclone2		2	1	1									
Cyclone3		2	2	1									
Stratix		2	1	1									
Stratix2		2	1	1									
Stratix3			2	1									
StratixGX		2	1	1									
Stratix2GX			2	1									
Max2		2	1	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FDPN

D-Type Flip-Flop with Asynchronous Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	1	1									
Cyclone2		2	1	1									
Cyclone3		2	2	1									
Stratix		2	1	1									
Stratix2		2	1	1									
Stratix3			2	1									
StratixGX		2	1	1									
Stratix2GX			2	1									
Max2		2	1	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FDR

D-Type Flip-Flop with Synchronous Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2	1										
XP		2	1	1									
XP2		2		1									

FDR_1

D-Type Negative Edge Flip-Flop with Synchronous Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2	1										
XP		2	1	1									
XP2		2		1									

FDRE

D-Type Flip-Flop with Clock Enable and Synchronous Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		2	2	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	1	1									
ECP		2	1	1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2	1										
XP		2	1	1									
XP2		2		1									

FDRE_1

D-Type Negative Edge Flip-Flop with Clock Enable and Synchronous Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		2	2	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	1	1									
ECP		2	1	1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2	1										
XP		2	1	1									
XP2		2		1									

FDREN

D-Type Flip-Flop with Clock Enable Synchronous Reset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		3	3	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		3											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	2	1									
ECP		4	2	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		4	2										
XP		4	2	1									
XP2		2	1	1									

FDRN

D-Type Flip-Flop with Synchronous Reset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		4	2										
XP		4	2	1									
XP2		2	1	1									

FDRS

D-Type Flip-Flop with Synchronous Reset and Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FDRS_1

D-Type Negative Edge Flip-Flop with Synchronous Reset and Set

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FDRSE

D-Type Flip-Flop with Synchronous Reset and Set and Clock Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2	1									
ECP		2	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		2	2										
XP		2	2	1									
XP2		4	2	1									

FDRSE_1

D-Type Negative Edge Flip-Flop with Synchronous Reset and Set and Clock Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2	1									
ECP		2	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		2	2										
XP		2	2	1									
XP2		4	2	1									

FDRSEN

D-Type Flip-Flop with Synchronous Reset and Set, Clock Enable and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		3	3	1									
Stratix2GX			2	1									
Max2		3	3	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		3											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3	1									
ECP		4	3	1									
ECP2		6	3	1									
ECP2M		6	3	1									
SC		4	3	1									
MACHXO		4	3										
XP		4	3	1									
XP2		6	3	1									

FDRSN

D-Type Flip-Flop with Synchronous Reset, Set and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		2		1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		2	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FDS

D-Type Flip-Flop with Synchronous Set, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2	1										
XP		2	1	1									
XP2		2		1									

FDS_1

D-Type Negative Edge Flip-Flop with Synchronous Set

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		2		1									
ECP2M		2		1									
SC		2		1									
MACHXO		2	1										
XP		2	1	1									
XP2		2		1									

FDSE

D-Type Flip-Flop with Clock Enable and Synchronous Set

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		2	2	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FDSE_1

D-Type Negative Edge Flip-Flop with Clock Enable and Synchronous Set

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		2	2	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1								1	
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FDSEN

D-Type Flip-Flop with Clock Enable Synchronous Set and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		3	3	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		3											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		2	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FDSN

D-Type Flip-Flop with Synchronous Set and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		1	1	1									
Spartan2E		1	1	1									
Spartan3		1	1	1									
Spartan3A		1	1	1									
Spartan3ADSP		1	1										
Spartan3AN		1	1										
Spartan3E		1	1	1									
Spartan3L		1	1	1									
Virtex		1	1	1									
Virtex2		1	1	1									
Virtex2p		1	1	1									
VirtexE		1	1	1									
Virtex4		3	1	1									
Virtex5		1	1										
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		4	2										
XP		4	2	1									
XP2		2	1	1									

FDSR

D-Type Flip-Flop with Synchronous Set and Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		3	2	1									
Spartan2E		3	2	1									
Spartan3		3	2	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2										
Spartan3AN		3	2										
Spartan3E		3	2	1								1	
Spartan3L		3	2	1									
Virtex		3	2	1									
Virtex2		3	2	1									
Virtex2p		3	2	1									
VirtexE		3	2	1									
Virtex4		3	2	1									
Virtex5		3	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		4	1	1									
ECP2M		4	1	1									
SC		4	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		4	1	1									

FDSR_1

D-Type Negative Edge Flip-Flop with Synchronous Set and Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		3	2	1									
Spartan2E		3	2	1									
Spartan3		3	2	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2										
Spartan3AN		3	2										
Spartan3E		3	2	1									
Spartan3L		3	2	1									
Virtex		3	2	1									
Virtex2		3	2	1									
Virtex2p		3	2	1									
VirtexE		3	2	1									
Virtex4		3	2	1									
Virtex5		3	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		1											
EC		2	1	1									
ECP		2	1	1									
ECP2		4	1	1									
ECP2M		4	1	1									
SC		4	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		4	1	1									

FDSRE

D-Type Flip-Flop with Synchronous Set and Reset and Clock Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		3	3	1									
Spartan2E		3	3	1									
Spartan3		3	3	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3										
Spartan3AN		3	3										
Spartan3E		3	3	1								1	
Spartan3L		3	3	1									
Virtex		3	3	1									
Virtex2		3	3	1									
Virtex2p		3	3	1									
VirtexE		3	3	1									
Virtex4		3	3	1									
Virtex5		3	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		2	2	1									
ECP		2	2	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	2										
XP		2	2	1									
XP2		2	1	1									

FDSRE_1

D-Type Negative Edge Flip-Flop with Synchronous Set and Reset and Clock Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		3	3	1									
Spartan2E		3	3	1									
Spartan3		3	3	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3										
Spartan3AN		3	3										
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		3	3	1									
Virtex2		3	3	1									
Virtex2p		3	3	1									
VirtexE		3	3	1									
Virtex4		3	3	1									
Virtex5		3	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		2	2	1									
ECP		2	2	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	2										
XP		2	2	1									
XP2		2	1	1									

FDSREN

D-Type Flip-Flop with Synchronous Set, Reset, Clock Enable and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		3	3	1									
Stratix2GX			2	1									
Max2		3	3	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		5											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	3	1									
ECP		4	3	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		2	2	1									
MACHXO		4	3										
XP		4	3	1									
XP2		4	2	1									

FDSRN

D-Type Flip-Flop with Synchronous Set, Reset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	1	1									
Spartan2E		2	1	1									
Spartan3		2	1	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2	1									
Spartan3AN		3	2	1									
Spartan3E		3	2	1									
Spartan3L		3	2	1									
Virtex		2	1	1									
Virtex2		2	1	1									
Virtex2p		2	1	1									
VirtexE		2	1	1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FJKC

J-K Flip-Flop with Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1								1	
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FJKC_1

J-K Negative Edge Flip-Flop with Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L													
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FJKCE

J-K Flip-Flop with Clock Enable and Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	1	1									
Spartan2E		2	1	1									
Spartan3		2	1	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2	1									
Spartan3AN		3	2	1									
Spartan3E		3	2	1								1	
Spartan3L		3	2	1									
Virtex		2	1	1									
Virtex2		2	1	1									
Virtex2p		2	1	1									
VirtexE		2	1	1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FJKCE_1

J-K Negative Edge Flip-Flop with Clock Enable and Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	1	1									
Spartan2E		2	1	1									
Spartan3		2	1	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2	1									
Spartan3AN		3	2	1									
Spartan3E		3	2	1									
Spartan3L		3	2	1									
Virtex		2	1	1									
Virtex2		2	1	1									
Virtex2p		2	1	1									
VirtexE		2	1	1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FJKCEN

J-K Flip-Flop with Clock Enable, Asynchronous Clear and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	1	1									
Spartan2E		2	1	1									
Spartan3		2	1	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2	1									
Spartan3AN		3	2	1									
Spartan3E		3	2	1									
Spartan3L		3	2	1									
Virtex		2	1	1									
Virtex2		2	1	1									
Virtex2p		2	1	1									
VirtexE		2	1	1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		3											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		2	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FJKCN

J-K Flip-Flop with Asynchronous Clear and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		3	3	1									
Stratix3			3	1									
StratixGX		3	3	1									
Stratix2GX			3	1									
Max2		3	3	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		6	3	1									
ECP		6	3	1									
ECP2		6	3	1									
ECP2M		6	3	1									
SC		4	3	1									
MACHXO		6	3										
XP		6	3	1									
XP2		6	3	1									

FJKCP

J-K Flip-Flop with Asynchronous Clear and Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		5	1	1									
Cyclone3		5	5	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			4	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1								1	
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		7											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		10	5	2									
ECP		10	5	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		10	5										
XP		10	5	2									
XP2		4	3	2									

FJKCP_1

J-K Negative Edge Flip-Flop with Asynchronous Clear and Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			4	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		7											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		10	5	2									
ECP		10	5	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		10	5										
XP		10	5	2									
XP2		4	3	2									

FJKCPE

J-K Flip-Flop with Asynchronous Clear and Preset and Clock Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		5	1	1									
Cyclone3		5	5	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			4	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	1	1									
Spartan2E		2	1	1									
Spartan3		2	1	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2	1									
Spartan3AN		3	2	1									
Spartan3E		3	2	1								1	
Spartan3L		3	2	1									
Virtex		2	1	1									
Virtex2		2	1	1									
Virtex2p		2	1	1									
VirtexE		2	1	1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		8	4	2									
ECP		8	4	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		8	4										
XP		8	4	2									
XP2		4	3	2									

FJKCPE_1

J-K Negative Edge Flip-Flop with Asynchronous Clear and Preset and Clock Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			4	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	1	1									
Spartan2E		2	1	1									
Spartan3		2	1	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2	1									
Spartan3AN		3	2	1									
Spartan3E		3	2	1									
Spartan3L		3	2	1									
Virtex		2	1	1									
Virtex2		2	1	1									
Virtex2p		2	1	1									
VirtexE		2	1	1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		8	4	2									
ECP		8	4	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		8	4										
XP		8	4	2									
XP2		4	3	2									

FJKCPEN

J-K Flip-Flop with Asynchronous Clear, Preset, Clock Enable and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			5	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		3	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	1	1									
Spartan2E		2	1	1									
Spartan3		2	1	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2	1									
Spartan3AN		3	2	1									
Spartan3E		3	2	1									
Spartan3L		3	2	1									
Virtex		2	1	1									
Virtex2		2	1	1									
Virtex2p		2	1	1									
VirtexE		2	1	1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		7											
ProAsic3E		7											
Fusion		7											
EC		10	5	2									
ECP		10	5	2									
ECP2		4	4	2									
ECP2M		4	4	2									
SC		6	4	3									
MACHXO		10	5										
XP		10	5	2									
XP2		4	4	2									

FJKCPN

J-K Flip-Flop with Asynchronous Clear, Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			5	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		3	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		7											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		12	6	2									
ECP		12	6	2									
ECP2		4	4	2									
ECP2M		4	4	2									
SC		6	4	3									
MACHXO		12	6										
XP		12	6	2									
XP2		4	4	2									

FJKP

J-K Flip-Flop with Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		3	3	1									
Stratix3			3	1									
StratixGX		3	3	1									
Stratix2GX			3	1									
Max2		3	3	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1								1	
Spartan3L													
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FJKP_1

J-K Negative Edge Flip-Flop with Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		3	3	1									
Stratix3			3	1									
StratixGX		3	3	1									
Stratix2GX			3	1									
Max2		3	3	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L													
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FJKPE

J-K Flip-Flop with Clock Enable and Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	1	1									
Spartan2E		2	1	1									
Spartan3		2	1	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2	1									
Spartan3AN		3	2	1									
Spartan3E		3	2	1								1	
Spartan3L													
Virtex		2	1	1									
Virtex2		2	1	1									
Virtex2p		2	1	1									
VirtexE		2	1	1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FJKPE_1

J-K Negative Edge Flip-Flop with Clock Enable and Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	1	1									
Spartan2E		2	1	1									
Spartan3		2	1	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2	1									
Spartan3AN		3	2	1									
Spartan3E		3	2	1									
Spartan3L													
Virtex		2	1	1									
Virtex2		2	1	1									
Virtex2p		2	1	1									
VirtexE		2	1	1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FJKPEN

J-K Flip-Flop with Clock Enable, Asynchronous Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	1	1									
Spartan2E		2	1	1									
Spartan3		2	1	1									
Spartan3A		3	2	1									
Spartan3ADSP		3	2	1									
Spartan3AN		3	2	1									
Spartan3E		3	2	1									
Spartan3L													
Virtex		2	1	1									
Virtex2		2	1	1									
Virtex2p		2	1	1									
VirtexE		2	1	1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		3											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		2	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FJKPN

J-K Flip-Flop with Asynchronous Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		3	3	1									
Stratix3			3	1									
StratixGX		3	3	1									
Stratix2GX			3	1									
Max2		3	3	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L													
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		6	3	1									
ECP		6	3	1									
ECP2		6	3	1									
ECP2M		6	3	1									
SC		4	3	1									
MACHXO		6	3										
XP		6	3	1									
XP2		6	3	1									

FJKRSE

J-K Flip-Flop with Clock Enable and Synchronous Reset and Set

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		2	2	1									
Cyclone3		4	4	1									
Stratix		3	3	1									
Stratix2		3	3	1									
Stratix3			2	1									
StratixGX		3	3	1									
Stratix2GX			1	1									
Max2		3	3	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		4	3	1									
Spartan2E		4	3	1									
Spartan3		4	3	1									
Spartan3A		5	4	1									
Spartan3ADSP		5	4	1									
Spartan3AN		5	4	1									
Spartan3E		5	4	1								1	
Spartan3L		5	4	1									
Virtex		4	3	1									
Virtex2		4	3	1									
Virtex2p		4	3	1									
VirtexE		4	3	1									
Virtex4		5	4	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		7											
ProAsic3		7											
ProAsic3E		6											
Fusion		6											
EC		2	2	1									
ECP		2	2	1									
ECP2		4	3	1									
ECP2M		4	3	1									
SC		4	3	1									
MACHXO		6	4										
XP		6	4	1									
XP2		4	3	1									

FJKRSE_1

J-K Negative Edge Flip-Flop with Clock Enable and Synchronous Reset and Set

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		2	2	1									
Cyclone3		4	4	1									
Stratix		3	3	1									
Stratix2		3	3	1									
Stratix3			2	1									
StratixGX		3	3	1									
Stratix2GX			1	1									
Max2		3	3	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		4	3	1									
Spartan2E		4	3	1									
Spartan3		4	3	1									
Spartan3A		5	4	1									
Spartan3ADSP		5	4	1									
Spartan3AN		5	4	1									
Spartan3E		5	4	1									
Spartan3L		5	4	1									
Virtex		4	3	1									
Virtex2		4	3	1									
Virtex2p		4	3	1									
VirtexE		4	3	1									
Virtex4		5	4	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		7											
ProAsic3		7											
ProAsic3E		6											
Fusion		6											
EC		2	2	1									
ECP		2	2	1									
ECP2		4	3	1									
ECP2M		4	3	1									
SC		4	3	1									
MACHXO		6	4										
XP		6	4	1									
XP2		4	3	1									

FJKRSEN

J-K Flip-Flop with Clock Enable, Synchronous Reset and Set and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		4	4	1									
Cyclone2		3	3	1									
Cyclone3		5	5	1									
Stratix		4	4	1									
Stratix2		4	4	1									
Stratix3			3	1									
StratixGX		4	4	1									
Stratix2GX			2	1									
Max2		4	4	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		4	3	1									
Spartan2E		4	3	1									
Spartan3		4	3	1									
Spartan3A		5	4	1									
Spartan3ADSP		5	4	1									
Spartan3AN		5	4	1									
Spartan3E		5	4	1									
Spartan3L		5	4	1									
Virtex		4	3	1									
Virtex2		4	3	1									
Virtex2p		4	3	1									
VirtexE		4	3	1									
Virtex4		5	4	1									
Virtex5		6	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		7											
ProAsic3		8											
ProAsic3E		7											
Fusion		7											
EC		4	3	1									
ECP		4	3	1									
ECP2		4	4	1									
ECP2M		4	4	1									
SC		6	4	1									
MACHXO		8	5										
XP		8	5	1									
XP2		4	4	1									

FJKSRE

J-K Flip-Flop with Clock Enable and Synchronous Set and Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		4	4	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1								1	
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		7											
ProAsic3		7											
ProAsic3E		7											
Fusion		7											
EC		2	2	1									
ECP		2	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		2	2										
XP		2	2	1									
XP2		4	2	1									

FJKSRE_1

J-K Negative Edge Flip-Flop with Clock Enable and Synchronous Set and Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		4	4	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		7											
ProAsic3		7											
ProAsic3E		7											
Fusion		7											
EC		2	2	1									
ECP		2	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		2	2										
XP		2	2	1									
XP2		4	2	1									

FJKSREN

J-K Flip-Flop with Clock Enable, Synchronous Set and Reset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		5	5	1									
Stratix		3	3	1									
Stratix2		2	2	1									
Stratix3			3	1									
StratixGX		3	3	1									
Stratix2GX			2	1									
Max2		3	3	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		7											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		4	3	1									
ECP		4	3	1									
ECP2		4	3	1									
ECP2M		4	3	1									
SC		4	3	1									
MACHXO		4	3										
XP		4	3	1									
XP2		4	3	1									

FTC

Toggle Flip-Flop with Toggle Enable and Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1								1	
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FTC_1

Negative Edge Toggle Flip-Flop with Toggle Enable and Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1									
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FTCE

Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1								1	
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	2	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		4	2										
XP		4	2	1									
XP2		2	1	1									

FTCE_1

Negative Edge Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		1	1	1									
Cyclone3		1	1	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		1	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1									
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	2	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		4	2										
XP		4	2	1									
XP2		2	1	1									

FTCEN

Toggle Flip-Flop with Toggle, Clock Enable, Asynchronous Clear and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1									
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		2	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FTCLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1								1	
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FTCLE_1

Toggle/Loadable Negative Edge Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FTCLEN

Toggle/Loadable Flip-Flop with Toggle, Clock Enable, Asynchronous Clear and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		2	2	1									
Stratix3			3	1									
StratixGX		3	3	1									
Stratix2GX			3	1									
Max2		3	3	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		6	3	1									
ECP		6	3	1									
ECP2		6	3	1									
ECP2M		6	3	1									
SC		4	3	1									
MACHXO		6	3										
XP		6	3	1									
XP2		6	3	1									

FTCN

Toggle Flip-Flop with Toggle Enable, Asynchronous Clear and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1									
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		2	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FTCP

Toggle Flip-Flop with Toggle Enable and Asynchronous Clear and Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		5	1	1									
Cyclone3		5	5	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			4	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1									
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		8	4	2									
ECP		8	4	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		8	4										
XP		8	4	2									
XP2		4	3	2									

FTCP_1

Negative Edge Toggle Flip-Flop with Toggle Enable and Asynchronous Clear and Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			4	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1									
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		8	4	2									
ECP		8	4	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		8	4										
XP		8	4	2									
XP2		4	3	2									

FTCPE

Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		5	1	1									
Cyclone3		5	5	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			4	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1									
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	2	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		6											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		8	4	2									
ECP		8	4	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		10	5										
XP		10	5	2									
XP2		4	3	2									

FTCPE_1

Negative Edge Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1	1	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		1	1	1									
Stratix2		1	1	1									
Stratix3			4	1									
StratixGX		1	1	1									
Stratix2GX			1	1									
Max2		2	1	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1									
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	2	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		6											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		8	4	2									
ECP		8	4	2									
ECP2		4	3	2									
ECP2M		4	3	2									
SC		6	3	3									
MACHXO		10	5										
XP		10	5	2									
XP2		4	3	2									

FTCPEN

Toggle Flip-Flop with Toggle, Clock Enable, Asynchronous Clear and Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			5	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		3	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1									
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		10	5	2									
ECP		10	5	2									
ECP2		4	4	2									
ECP2M		4	4	2									
SC		6	4	3									
MACHXO		10	5										
XP		10	5	2									
XP2		4	4	2									

FTCPLE

Loadable Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	2	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			6	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		3	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		7											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		10	5	2									
ECP		10	5	2									
ECP2		4	4	2									
ECP2M		4	4	2									
SC		6	4	3									
MACHXO		10	5										
XP		10	5	2									
XP2		4	4	2									

FTCPLE_1

Loadable Negative Edge Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	2	1									
Cyclone2		7	3	1									
Cyclone3		7	7	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			6	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		3	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		7											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		10	5	2									
ECP		10	5	2									
ECP2		4	4	2									
ECP2M		4	4	2									
SC		6	4	3									
MACHXO		10	5										
XP		10	5	2									
XP2		4	4	2									

FTCPLEN

Loadable Toggle Flip-Flop with Toggle, Clock Enable, Asynchronous Clear and Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		7	3	1									
Cyclone3		7	7	1									
Stratix		3	3	1									
Stratix2		2	2	1									
Stratix3			7	1									
StratixGX		3	3	1									
Stratix2GX			2	1									
Max2		4	3	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		7											
ProAsic3		7											
ProAsic3E		7											
Fusion		7											
EC		12	6	2									
ECP		12	6	2									
ECP2		6	5	2									
ECP2M		6	5	2									
SC		6	5	3									
MACHXO		12	6										
XP		12	6	2									
XP2		6	5	2									

FTCPN

Toggle Flip-Flop with Toggle Enable, Asynchronous Clear, Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		6	2	1									
Cyclone3		6	6	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			5	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		3	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1									
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		5											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		10	5	2									
ECP		10	5	2									
ECP2		4	4	2									
ECP2M		4	4	2									
SC		6	4	3									
MACHXO		10	5										
XP		10	5	2									
XP2		4	4	2									

FTP

Toggle Flip-Flop with Toggle Enable and Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1								1	
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FTP_1

Negative Edge Toggle Flip-Flop with Toggle Enable and Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1									
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

FTPE

Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1								1	
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	2	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		4	2										
XP		4	2	1									
XP2		2	1	1									

FTPE_1

Negative Edge Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1									
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	2	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		3											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		4	2										
XP		4	2	1									
XP2		2	1	1									

FTPEN

Toggle Flip-Flop with Toggle, Clock Enable, Asynchronous Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1									
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		2	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FTPLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		2	2	1									
Stratix3			3	1									
StratixGX		3	3	1									
Stratix2GX			3	1									
Max2		3	3	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1								1	
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FTPLE_1

Toggle/Loadable Negative Edge Flip-Flop with Toggle and Clock Enable and Asynchronous Preset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		2	2	1									
Stratix3			3	1									
StratixGX		3	3	1									
Stratix2GX			3	1									
Max2		3	3	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FTPLEN

Toggle/Loadable Flip-Flop with Toggle, Clock Enable, Asynchronous Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		2	2	1									
Stratix3			3	1									
StratixGX		3	3	1									
Stratix2GX			3	1									
Max2		3	3	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		6	3	1									
ECP		6	3	1									
ECP2		6	3	1									
ECP2M		6	3	1									
SC		4	3	1									
MACHXO		6	3										
XP		6	3	1									
XP2		6	3	1									

FTPN

Toggle Flip-Flop with Toggle Enable, Asynchronous Preset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			2	1									
Max2		2	2	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1									
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	2	1									
Virtex5		2	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		2											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	2	1									
ECP		4	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		2	2	1									
MACHXO		4	2										
XP		4	2	1									
XP2		4	2	1									

FTRSE

Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1								1	
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	2	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2	1									
ECP		2	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		2	2										
XP		2	2	1									
XP2		4	2	1									

FTRSE_1

Negative Edge Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			1	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1									
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	2	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		4											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2	1									
ECP		2	2	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		2	2										
XP		2	2	1									
XP2		4	2	1									

FTRSEN

Toggle Flip-Flop with Toggle, Clock Enable, Synchronous Reset and Set and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		2	2	1									
Stratix3			2	1									
StratixGX		3	3	1									
Stratix2GX			2	1									
Max2		3	3	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		4	1	1									
Spartan2E		4	1	1									
Spartan3		4	1	1									
Spartan3A		5	2	1									
Spartan3ADSP		5	2	1									
Spartan3AN		5	2	1									
Spartan3E		5	2	1									
Spartan3L		5	2	1									
Virtex		4	1	1									
Virtex2		4	1	1									
Virtex2p		4	1	1									
VirtexE		4	1	1									
Virtex4		5	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3	1									
ECP		4	3	1									
ECP2		6	3	1									
ECP2M		6	3	1									
SC		4	3	1									
MACHXO		4	3										
XP		4	3	1									
XP2		6	3	1									

FTRSLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		4	4	1									
Stratix		3	3	1									
Stratix2		1	1	1									
Stratix3			2	1									
StratixGX		3	3	1									
Stratix2GX			2	1									
Max2		3	3	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1								1	
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		5											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3	1									
ECP		4	3	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	3										
XP		4	3	1									
XP2		4	2	1									

FTRSLE_1

Toggle/Loadable Negative Edge Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		4	4	1									
Stratix		3	3	1									
Stratix2		1	1	1									
Stratix3			2	1									
StratixGX		3	3	1									
Stratix2GX			2	1									
Max2		3	3	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		5											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	3	1									
ECP		4	3	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	3										
XP		4	3	1									
XP2		4	2	1									

FTRSLEN

Toggle/Loadable Flip-Flop with Toggle, Clock Enable, Synchronous Reset and Set and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		4	4	1									
Cyclone2		4	4	1									
Cyclone3		5	5	1									
Stratix		4	4	1									
Stratix2		2	2	1									
Stratix3			3	1									
StratixGX		4	4	1									
Stratix2GX			3	1									
Max2		4	4	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		6	4	1									
ECP		6	4	1									
ECP2		6	3	1									
ECP2M		6	3	1									
SC		4	3	1									
MACHXO		6	4										
XP		6	4	1									
XP2		6	3	1									

FTSRE

Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1								1	
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		4											
Fusion		4											
EC		2	2	1									
ECP		2	2	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	2										
XP		2	2	1									
XP2		2	1	1									

FTSRE_1

Negative Edge Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		2	2	1									
Cyclone2		2	2	1									
Cyclone3		2	2	1									
Stratix		2	2	1									
Stratix2		1	1	1									
Stratix3			2	1									
StratixGX		2	2	1									
Stratix2GX			1	1									
Max2		2	2	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		5											
ProAsic3		5											
ProAsic3E		4											
Fusion		4											
EC		2	2	1									
ECP		2	2	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	2										
XP		2	2	1									
XP2		2	1	1									

FTSREN

Toggle Flip-Flop with Toggle, Clock Enable, Synchronous Set and Reset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		3	3	1									
Stratix		3	3	1									
Stratix2		2	2	1									
Stratix3			3	1									
StratixGX		3	3	1									
Stratix2GX			2	1									
Max2		3	3	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		5											
ProAsic3		6											
ProAsic3E		5											
Fusion		5											
EC		4	3	1									
ECP		4	3	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		2	2	1									
MACHXO		4	3										
XP		4	3	1									
XP2		4	2	1									

FTSRLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		4	4	1									
Stratix		3	3	1									
Stratix2		1	1	1									
Stratix3			2	1									
StratixGX		3	3	1									
Stratix2GX			1	1									
Max2		3	3	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1								1	
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		8											
ProAsic3		7											
ProAsic3E		7											
Fusion		7											
EC		4	3	1									
ECP		4	3	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	3										
XP		4	3	1									
XP2		4	2	1									

FTSRLE_1

Toggle/Loadable Negative Edge Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	1									
Cyclone		3	3	1									
Cyclone2		3	3	1									
Cyclone3		4	4	1									
Stratix		3	3	1									
Stratix2		1	1	1									
Stratix3			2	1									
StratixGX		3	3	1									
Stratix2GX			1	1									
Max2		3	3	1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		8											
ProAsic3		7											
ProAsic3E		7											
Fusion		7											
EC		4	3	1									
ECP		4	3	1									
ECP2		4	2	1									
ECP2M		4	2	1									
SC		4	2	1									
MACHXO		4	3										
XP		4	3	1									
XP2		4	2	1									

FTSRLEN

Toggle/Loadable Flip-Flop with Toggle, Clock Enable, Synchronous Set and Reset and Inverted and Non-Inverted Outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		4	4	1									
Cyclone2		4	4	1									
Cyclone3		5	5	1									
Stratix		4	4	1									
Stratix2		2	2	1									
Stratix3			3	1									
StratixGX		4	4	1									
Stratix2GX			2	1									
Max2		4	4	1									
Max3000a	2	2		1									
Max7000b	2	2		1									
Max7000ae	2	2		1									
Max7000s	2	2		1									
Spartan2		2	2	1									
Spartan2E		2	2	1									
Spartan3		2	2	1									
Spartan3A		3	3	1									
Spartan3ADSP		3	3	1									
Spartan3AN		3	3	1									
Spartan3E		3	3	1									
Spartan3L		3	3	1									
Virtex		2	2	1									
Virtex2		2	2	1									
Virtex2p		2	2	1									
VirtexE		2	2	1									
Virtex4		3	3	1									
Virtex5		4	1	1									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		6	4	1									
ECP		6	4	1									
ECP2		4	3	1									
ECP2M		4	3	1									
SC		4	3	1									
MACHXO		4	4										
XP		4	4	1									
XP2		4	3	1									

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1