FPGA Encoder Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Encoder cores.

Core Reference
CR0132 (v1.11) December 19, 2008

Encoder

The available Encoder cores are listed as follows:

E4_2B	*E4_2EB*	*E4_2ES*	*E4_2S*
E8_3B	*E8_3EB*	*E8_3ES*	*E8_3S*
E10_4B	*E10_4EB*	*E10_4ES*	*E10_4S*
E16_4B	*E16_4EB*	*E16_4ES*	*E16_4S*
E32_5B	*E32_5EB*		

E4_2B

4- to 2-Bit Priority Encoder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		4											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4	2										
ECP		4	2										
ECP2		4	2										
ECP2M		4	2										
SC		4	2										
MACHXO		4	2										
XP		4	2										
XP2		4	2										

E4_2EB

4- to 2-Bit Priority Encoder with Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		4											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

E4_2ES

4- to 2-Bit Priority Encoder with Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		4											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

E4_2S

4- to 2-Bit Priority Encoder, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		4											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		2											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		4	2										
ECP		4	2										
ECP2		4	2										
ECP2M		4	2										
SC		4	2										
MACHXO		4	2										
XP		4	2										
XP2		4	2										

E8_3B

8- to 3-Bit Priority Encoder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			5										
Max2		5	5										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		8	7										
Spartan2E		8	7										
Spartan3		10	8										
Spartan3A		8	8										
Spartan3ADSP		6	6										
Spartan3AN		8	8										
Spartan3E		8	7										
Spartan3L		6	6										
Virtex		8	7										
Virtex2		8	7										
Virtex2p		8	7										
VirtexE		8	7										
Virtex4		10	8										
Virtex5		6											
CoolRunner2	3												
CoolRunnerXpla3	3												
Xc9500	3												
Xc9500XL	3												
Xc9500XV	3												
ProAsicPlus		9											
ProAsic3		10											
ProAsic3E		9											
Fusion		10											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
SC		6	6										
MACHXO		6	6										
XP		6	6										
XP2		6	6										

E8_3EB

8- to 3-Bit Priority Encoder with Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6										
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		9	9										
Stratix		7	7										
Stratix2		5	5										
Stratix3			6										
StratixGX		7	7										
Stratix2GX			6										
Max2		7	7										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		10	8										
Spartan2E		10	8										
Spartan3		10	8										
Spartan3A		10	8										
Spartan3ADSP		10	9										
Spartan3AN		10	8										
Spartan3E		10	8										
Spartan3L		10	9										
Virtex		10	8										
Virtex2		10	8										
Virtex2p		10	8										
VirtexE		10	8										
Virtex4		10	8										
Virtex5		6											
CoolRunner2	3												
CoolRunnerXpla3	3												
Xc9500	3												
Xc9500XL	3												
Xc9500XV	3												
ProAsicPlus		11											
ProAsic3		12											
ProAsic3E		10											
Fusion		10											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
SC		10	8										
MACHXO		8	8										
XP		8	8										
XP2		8	8										

E8_3ES

8- to 3-Bit Priority Encoder with Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6										
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		9	9										
Stratix		7	7										
Stratix2		6	6										
Stratix3			6										
StratixGX		7	7										
Stratix2GX			6										
Max2		7	7										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		10	8										
Spartan2E		10	8										
Spartan3		10	8										
Spartan3A		10	8										
Spartan3ADSP		10	9										
Spartan3AN		10	8										
Spartan3E		10	8										
Spartan3L		10	9										
Virtex		10	8										
Virtex2		10	8										
Virtex2p		10	8										
VirtexE		10	8										
Virtex4		10	8										
Virtex5		6											
CoolRunner2	3												
CoolRunnerXpla3	3												
Xc9500	3												
Xc9500XL	3												
Xc9500XV	3												
ProAsicPlus		11											
ProAsic3		13											
ProAsic3E		10											
Fusion		10											
EC		10	9										
ECP		10	9										
ECP2		8	8										
ECP2M		8	8										
SC		10	8										
MACHXO		8	8										
XP		8	8										
XP2		8	8										

E8_3S

8- to 3-Bit Priority Encoder, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			5										
Max2		5	5										
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		8	7										
Spartan2E		8	7										
Spartan3		10	8										
Spartan3A		8	8										
Spartan3ADSP		6	6										
Spartan3AN		8	8										
Spartan3E		8	7										
Spartan3L		6	6										
Virtex		8	7										
Virtex2		8	7										
Virtex2p		8	7										
VirtexE		8	7										
Virtex4		10	8										
Virtex5		6											
CoolRunner2	3												
CoolRunnerXpla3	3												
Xc9500	3												
Xc9500XL	3												
Xc9500XV	3												
ProAsicPlus		9											
ProAsic3		10											
ProAsic3E		9											
Fusion		10											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
SC		6	6										
MACHXO		6	6										
XP		6	6										
XP2		6	6										

E10_4B

Binary-Coded-Decimal (BCD) Encoder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			15										
Cyclone		22	22										
Cyclone2		22	22										
Cyclone3		25	25										
Stratix		21	21										
Stratix2		18	18										
Stratix3			17										
StratixGX		21	21										
Stratix2GX			10										
Max2		20	20										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		24	21										
Spartan2E		24	21										
Spartan3		22	21										
Spartan3A		22	21										
Spartan3ADSP		22	21										
Spartan3AN		22	21										
Spartan3E		24	21										
Spartan3L		22	20										
Virtex		24	21										
Virtex2		22	21										
Virtex2p		22	21										
VirtexE		24	21										
Virtex4		22	21										
Virtex5		10											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		37											
ProAsic3		36											
ProAsic3E		41											
Fusion		30											
EC		24	24										
ECP		24	24										
ECP2		20	20										
ECP2M		20	20										
SC		22	20										
MACHXO		22	21										
XP		26	26										
XP2		20	20										

E10_4EB

Binary-Coded-Decimal (BCD) Encoder with Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			15										
Cyclone		17	17										
Cyclone2		17	17										
Cyclone3		28	28										
Stratix		24	24										
Stratix2		18	18										
Stratix3			17										
StratixGX		24	24										
Stratix2GX			12										
Max2		22	22										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		26	23										
Spartan2E		26	23										
Spartan3		26	23										
Spartan3A		24	22										
Spartan3ADSP		24	22										
Spartan3AN		24	22										
Spartan3E		24	23										
Spartan3L		24	22										
Virtex		26	23										
Virtex2		26	23										
Virtex2p		26	23										
VirtexE		26	23										
Virtex4		24	23										
Virtex5		10											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		38											
ProAsic3		38											
ProAsic3E		39											
Fusion		33											
EC		22	22										
ECP		22	22										
ECP2		22	22										
ECP2M		22	22										
SC		24	22										
MACHXO		22	22										
XP		26	26										
XP2		22	21										

E10_4ES

Binary-Coded-Decimal (BCD) Encoder with Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			17										
Cyclone		20	20										
Cyclone2		20	20										
Cyclone3		25	25										
Stratix		17	17										
Stratix2		18	18										
Stratix3			17										
StratixGX		17	17										
Stratix2GX			12										
Max2		19	19										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		26	24										
Spartan2E		26	24										
Spartan3		26	24										
Spartan3A		22	21										
Spartan3ADSP		24	22										
Spartan3AN		22	21										
Spartan3E		24	23										
Spartan3L		24	22										
Virtex		26	24										
Virtex2		26	24										
Virtex2p		26	24										
VirtexE		26	24										
Virtex4		26	24										
Virtex5		12											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		33											
ProAsic3		32											
ProAsic3E		39											
Fusion		31											
EC		20	20										
ECP		20	20										
ECP2		22	22										
ECP2M		22	22										
SC		24	22										
MACHXO		22	21										
XP		22	21										
XP2		22	21										

E10_4S

Binary-Coded-Decimal (BCD) Encoder, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16										
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		25	25										
Stratix		19	19										
Stratix2		18	18										
Stratix3			14										
StratixGX		19	19										
Stratix2GX			10										
Max2		21	21										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		22	20										
Spartan2E		22	20										
Spartan3		24	20										
Spartan3A		22	19										
Spartan3ADSP		24	21										
Spartan3AN		22	19										
Spartan3E		22	20										
Spartan3L		22	20										
Virtex		22	20										
Virtex2		24	20										
Virtex2p		24	20										
VirtexE		22	20										
Virtex4		24	20										
Virtex5		10											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		32											
ProAsic3		31											
ProAsic3E		33											
Fusion		29											
EC		20	19										
ECP		20	19										
ECP2		20	20										
ECP2M		20	20										
SC		22	20										
MACHXO		20	19										
XP		20	20										
XP2		20	20										

E16_4B

16- to 4-Bit Priority Encoder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			12										
Cyclone		17	17										
Cyclone2		16	16										
Cyclone3		15	15										
Stratix		17	17										
Stratix2		14	14										
Stratix3			12										
StratixGX		17	17										
Stratix2GX			12										
Max2		17	17										
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		14	12										
Spartan2E		14	12										
Spartan3		14	12										
Spartan3A		14	12										
Spartan3ADSP		14	12										
Spartan3AN		14	12										
Spartan3E		14	12										
Spartan3L		14	12										
Virtex		14	12										
Virtex2		14	12										
Virtex2p		14	12										
VirtexE		14	12										
Virtex4		14	12										
Virtex5		12											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		25											
ProAsic3		28											
ProAsic3E		25											
Fusion		28											
EC		18	17										
ECP		18	17										
ECP2		16	13										
ECP2M		16	13										
SC		16	13										
MACHXO		14	13										
XP		14	13										
XP2		16	13										

E16_4EB

16- to 4-Bit Priority Encoder with Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			13										
Cyclone		18	18										
Cyclone2		18	18										
Cyclone3		16	16										
Stratix		18	18										
Stratix2		16	16										
Stratix3			13										
StratixGX		18	18										
Stratix2GX			13										
Max2		18	18										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		18	15										
Spartan2E		18	15										
Spartan3		18	15										
Spartan3A		18	15										
Spartan3ADSP		18	15										
Spartan3AN		18	15										
Spartan3E		18	15										
Spartan3L		18	15										
Virtex		18	15										
Virtex2		18	15										
Virtex2p		18	15										
VirtexE		18	15										
Virtex4		18	15										
Virtex5		16											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		28											
ProAsic3		32											
ProAsic3E		27											
Fusion		26											
EC		20	19										
ECP		20	19										
ECP2		16	15										
ECP2M		16	15										
SC		20	15										
MACHXO		16	15										
XP		16	15										
XP2		16	15										

E16_4ES

16- to 4-Bit Priority Encoder with Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			13										
Cyclone		18	18										
Cyclone2		20	20										
Cyclone3		16	16										
Stratix		18	18										
Stratix2		15	15										
Stratix3			13										
StratixGX		18	18										
Stratix2GX			13										
Max2		18	18										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		18	15										
Spartan2E		18	15										
Spartan3		18	15										
Spartan3A		18	15										
Spartan3ADSP		18	15										
Spartan3AN		18	15										
Spartan3E		18	15										
Spartan3L		18	15										
Virtex		18	15										
Virtex2		18	15										
Virtex2p		18	15										
VirtexE		18	15										
Virtex4		18	15										
Virtex5		12											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		29											
ProAsic3		32											
ProAsic3E		25											
Fusion		26											
EC		20	19										
ECP		20	19										
ECP2		16	15										
ECP2M		16	15										
SC		20	15										
MACHXO		16	15										
XP		16	15										
XP2		16	15										

E16_4S

16- to 4-Bit Priority Encoder, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			12										
Cyclone		17	17										
Cyclone2		16	16										
Cyclone3		15	15										
Stratix		17	17										
Stratix2		14	14										
Stratix3			12										
StratixGX		17	17										
Stratix2GX			12										
Max2		17	17										
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		14	12										
Spartan2E		14	12										
Spartan3		14	12										
Spartan3A		14	12										
Spartan3ADSP		14	12										
Spartan3AN		14	12										
Spartan3E		14	12										
Spartan3L		14	12										
Virtex		14	12										
Virtex2		14	12										
Virtex2p		14	12										
VirtexE		14	12										
Virtex4		14	12										
Virtex5		12											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		25											
ProAsic3		28											
ProAsic3E		25											
Fusion		27											
EC		18	17										
ECP		18	17										
ECP2		16	13										
ECP2M		16	13										
SC		16	13										
MACHXO		14	13										
XP		14	13										
XP2		16	13										

E32_5B

32- to 5-Bit Priority Encoder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			22										
Cyclone		56	56										
Cyclone2		52	52										
Cyclone3		37	37										
Stratix		56	56										
Stratix2		41	41										
Stratix3			39										
StratixGX		56	56										
Stratix2GX			27										
Max2		48	48										
Max3000a	13	13											
Max7000b	13	13											
Max7000ae	13	13											
Max7000s	13	13											
Spartan2		32	29										
Spartan2E		32	29										
Spartan3		34	27										
Spartan3A		32	27										
Spartan3ADSP		30	27										
Spartan3AN		32	27										
Spartan3E		34	27										
Spartan3L		32	27										
Virtex		32	29										
Virtex2		34	27										
Virtex2p		34	27										
VirtexE		32	29										
Virtex4		34	27										
Virtex5		34											
CoolRunner2	8												
CoolRunnerXpla3	6												
Xc9500	5												
Xc9500XL	5												
Xc9500XV	5												
ProAsicPlus		65											
ProAsic3		74											
ProAsic3E		69											
Fusion		64											
EC		54	54										
ECP		54	54										
ECP2		32	28										
ECP2M		32	28										
SC		34	28										
MACHXO		32	28										
XP		32	28										
XP2		34	28										

E32_5EB

32- to 5-Bit Priority Encoder with Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			25										
Cyclone		51	51										
Cyclone2		54	54										
Cyclone3		38	38										
Stratix		51	51										
Stratix2		38	38										
Stratix3			43										
StratixGX		51	51										
Stratix2GX			30										
Max2		53	53										
Max3000a	14	14											
Max7000b	14	14											
Max7000ae	14	14											
Max7000s	14	14											
Spartan2		38	31										
Spartan2E		38	31										
Spartan3		36	31										
Spartan3A		36	31										
Spartan3ADSP		38	31										
Spartan3AN		36	31										
Spartan3E		36	31										
Spartan3L		38	31										
Virtex		38	31										
Virtex2		36	31										
Virtex2p		36	31										
VirtexE		38	31										
Virtex4		36	31										
Virtex5		34											
CoolRunner2	9												
CoolRunnerXpla3	7												
Xc9500	5												
Xc9500XL	5												
Xc9500XV	5												
ProAsicPlus		75											
ProAsic3		81											
ProAsic3E		72											
Fusion		69											
EC		72	71										
ECP		72	71										
ECP2		36	31										
ECP2M		36	31										
SC		42	31										
MACHXO		36	31										
XP		36	31										
XP2		36	31										

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1