FPGA Decoder Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Decoder cores.

Core Reference
CR0131 (v1.11) December 19, 2008

Decoder

The available Decoder cores are listed as follows:

D2_4B	*D2_4EB*	*D2_4ES*	*D2_4S*
D3_8B	*D3_8EB*	*D3_8ES*	*D3_8S*
D4_10B	*D4_10EB*	*D4_10ES*	*D4_10S*
D4_16B	*D4_16EB*	*D4_16ES*	*D4_16S*
D5_32B	*D5_32EB*	*D7SEGB*	*D7SEGNB*
D7SEGNS	*D7SEGS*		

D2_4B

Binary 2- to 4-Bit Decoder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			4										
StratixGX		4	4										
Stratix2GX			4										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		8	4										
ECP		8	4										
ECP2		8	4										
ECP2M		8	4										
SC		8	4										
MACHXO		8	4										
XP		8	4										
XP2		8	4										

D2_4EB

Binary 2- to 4-Bit Decoder with Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			4										
StratixGX		4	4										
Stratix2GX			4										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		6											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

D2_4ES

Binary 2- to 4-Bit Decoder with Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			4										
StratixGX		4	4										
Stratix2GX			4										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		6											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
SC		4	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

D2_4S

Binary 2- to 4-Bit Decoder, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			4										
StratixGX		4	4										
Stratix2GX			4										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		4											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		8	4										
ECP		8	4										
ECP2		8	4										
ECP2M		8	4										
SC		8	4										
MACHXO		8	4										
XP		8	4										
XP2		8	4										

D3_8B

Binary 3- to 8-Bit Decoder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8										
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3			8										
StratixGX		8	8										
Stratix2GX			8										
Max2		8	8										
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8											
CoolRunner2	8												
CoolRunnerXpla3	8												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		12											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
SC		8	8										
MACHXO		8	8										
XP		8	8										
XP2		8	8										

D3_8EB

Binary 3- to 8-Bit Decoder with Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8										
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3			8										
StratixGX		8	8										
Stratix2GX			8										
Max2		8	8										
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8											
CoolRunner2	8												
CoolRunnerXpla3	8												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		14											
ProAsic3		14											
ProAsic3E		10											
Fusion		10											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
SC		8	8										
MACHXO		8	8										
XP		8	8										
XP2		8	8										

D3_8ES

Binary 3- to 8-Bit Decoder with Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8										
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3			8										
StratixGX		8	8										
Stratix2GX			8										
Max2		8	8										
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8											
CoolRunner2	8												
CoolRunnerXpla3	8												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		14											
ProAsic3		14											
ProAsic3E		10											
Fusion		10											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
SC		8	8										
MACHXO		8	8										
XP		8	8										
XP2		8	8										

D3_8S

Binary 3- to 8-Bit Decoder, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8										
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3			8										
StratixGX		8	8										
Stratix2GX			8										
Max2		8	8										
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8											
CoolRunner2	8												
CoolRunnerXpla3	8												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		12											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
SC		8	8										
MACHXO		8	8										
XP		8	8										
XP2		8	8										

D4_10B

Binary-Coded-Decimal (BCD) Decoder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10										
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3			10										
StratixGX		10	10										
Stratix2GX			10										
Max2		10	10										
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10	10										
Spartan3ADSP		10	10										
Spartan3AN		10	10										
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		8											
CoolRunner2	10												
CoolRunnerXpla3	10												
Xc9500	10												
Xc9500XL	10												
Xc9500XV	10												
ProAsicPlus		16											
ProAsic3		18											
ProAsic3E		13											
Fusion		13											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
SC		10	10										
MACHXO		10	10										
XP		10	10										
XP2		10	10										

D4_10EB

Binary-Coded-Decimal (BCD) Decoder with Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10										
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		20	20										
Stratix		12	12										
Stratix2		10	10										
Stratix3			10										
StratixGX		12	12										
Stratix2GX			10										
Max2		12	12										
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12	12										
Spartan3ADSP		12	12										
Spartan3AN		12	12										
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		8											
CoolRunner2	10												
CoolRunnerXpla3	10												
Xc9500	10												
Xc9500XL	10												
Xc9500XV	10												
ProAsicPlus		18											
ProAsic3		17											
ProAsic3E		15											
Fusion		14											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
SC		14	12										
MACHXO		12	12										
XP		12	12										
XP2													

D4_10ES

Binary-Coded-Decimal (BCD) Decoder with Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10										
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		20	20										
Stratix		12	12										
Stratix2		10	10										
Stratix3			10										
StratixGX		12	12										
Stratix2GX			10										
Max2		12	12										
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12	12										
Spartan3ADSP		12	12										
Spartan3AN		12	12										
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		6											
CoolRunner2	10												
CoolRunnerXpla3	10												
Xc9500	10												
Xc9500XL	10												
Xc9500XV	10												
ProAsicPlus		18											
ProAsic3		17											
ProAsic3E		13											
Fusion		14											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
SC		14	12										
MACHXO		12	12										
XP		12	12										
XP2		12	12										

D4_10S

Binary-Coded-Decimal (BCD) Decoder, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10										
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3			10										
StratixGX		10	10										
Stratix2GX			10										
Max2		10	10										
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10	10										
Spartan3ADSP		10	10										
Spartan3AN		10	10										
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		8											
CoolRunner2	10												
CoolRunnerXpla3	10												
Xc9500	10												
Xc9500XL	10												
Xc9500XV	10												
ProAsicPlus		17											
ProAsic3		18											
ProAsic3E		13											
Fusion		13											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
SC		10	10										
MACHXO		10	10										
XP		10	10										
XP2		10	10										

D4_16B

Binary 4- to 16-Bit Decoder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16										
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3			16										
StratixGX		16	16										
Stratix2GX			16										
Max2		16	16										
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16	16										
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		12											
CoolRunner2	16												
CoolRunnerXpla3	16												
Xc9500	16												
Xc9500XL	16												
Xc9500XV	16												
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		22											
Fusion		21											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
SC		16	16										
MACHXO		16	16										
XP		16	16										
XP2		16	16										

D4_16EB

Binary 4- to 16-Bit Decoder with Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16										
Cyclone		18	18										
Cyclone2		18	18										
Cyclone3		32	32										
Stratix		18	18										
Stratix2		16	16										
Stratix3			16										
StratixGX		18	18										
Stratix2GX			16										
Max2		18	18										
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		18	18										
Spartan2E		18	18										
Spartan3		18	18										
Spartan3A		18	18										
Spartan3ADSP		18	18										
Spartan3AN		18	18										
Spartan3E		18	18										
Spartan3L		18	18										
Virtex		18	18										
Virtex2		18	18										
Virtex2p		18	18										
VirtexE		18	18										
Virtex4		18	18										
Virtex5		14											
CoolRunner2	16												
CoolRunnerXpla3	16												
Xc9500	16												
Xc9500XL	16												
Xc9500XV	16												
ProAsicPlus		26											
ProAsic3		24											
ProAsic3E		22											
Fusion		22											
EC		18	18										
ECP		18	18										
ECP2		18	18										
ECP2M		18	18										
SC		18	18										
MACHXO		18	18										
XP		18	18										
XP2		18	18										

D4_16ES

Binary 4- to 16-Bit Decoder with Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16										
Cyclone		18	18										
Cyclone2		18	18										
Cyclone3		32	32										
Stratix		18	18										
Stratix2		16	16										
Stratix3			16										
StratixGX		18	18										
Stratix2GX			16										
Max2		18	18										
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		18	18										
Spartan2E		18	18										
Spartan3		18	18										
Spartan3A		18	18										
Spartan3ADSP		18	18										
Spartan3AN		18	18										
Spartan3E		18	18										
Spartan3L		18	18										
Virtex		18	18										
Virtex2		18	18										
Virtex2p		18	18										
VirtexE		18	18										
Virtex4		18	18										
Virtex5		12											
CoolRunner2	16												
CoolRunnerXpla3	16												
Xc9500	16												
Xc9500XL	16												
Xc9500XV	16												
ProAsicPlus		26											
ProAsic3		24											
ProAsic3E		22											
Fusion		22											
EC		18	18										
ECP		18	18										
ECP2		18	18										
ECP2M		18	18										
SC		18	18										
MACHXO		18	18										
XP		18	18										
XP2		18	18										

D4_16S

Binary 4- to 16-Bit Decoder, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			16										
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3			16										
StratixGX		16	16										
Stratix2GX			16										
Max2		16	16										
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16	16										
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		14											
CoolRunner2	16												
CoolRunnerXpla3	16												
Xc9500	16												
Xc9500XL	16												
Xc9500XV	16												
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		22											
Fusion		21											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
SC		16	16										
MACHXO		16	16										
XP		16	16										
XP2		16	16										

D5_32B

Binary 5- to 32-Bit Decoder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32										
Cyclone		36	36										
Cyclone2		36	36										
Cyclone3		36	36										
Stratix		36	36										
Stratix2		32	32										
Stratix3			32										
StratixGX		36	36										
Stratix2GX			32										
Max2		36	36										
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		36	36										
Spartan2E		36	36										
Spartan3		36	36										
Spartan3A		36	36										
Spartan3ADSP		36	36										
Spartan3AN		36	36										
Spartan3E		36	36										
Spartan3L		36	36										
Virtex		36	36										
Virtex2		36	36										
Virtex2p		36	36										
VirtexE		36	36										
Virtex4		36	36										
Virtex5		28											
CoolRunner2	32												
CoolRunnerXpla3	32												
Xc9500	32												
Xc9500XL	32												
Xc9500XV	32												
ProAsicPlus		48											
ProAsic3		44											
ProAsic3E		44											
Fusion		40											
EC		64	64										
ECP		64	64										
ECP2		36	36										
ECP2M		36	36										
SC		36	36										
MACHXO		38	37										
XP		36	36										
XP2		36	36										

D5_32EB

Binary 5- to 32-Bit Decoder with Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32										
Cyclone		38	38										
Cyclone2		40	40										
Cyclone3		36	36										
Stratix		38	38										
Stratix2		64	64										
Stratix3			32										
StratixGX		38	38										
Stratix2GX			32										
Max2		38	38										
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		38	38										
Spartan2E		38	38										
Spartan3		38	38										
Spartan3A		36	36										
Spartan3ADSP		36	36										
Spartan3AN		36	36										
Spartan3E		38	38										
Spartan3L		36	36										
Virtex		38	38										
Virtex2		38	38										
Virtex2p		38	38										
VirtexE		38	38										
Virtex4		38	38										
Virtex5		38											
CoolRunner2	32												
CoolRunnerXpla3	32												
Xc9500	32												
Xc9500XL	32												
Xc9500XV	32												
ProAsicPlus		50											
ProAsic3		42											
ProAsic3E		44											
Fusion		46											
EC		128	96										
ECP		128	96										
ECP2		36	36										
ECP2M		36	36										
SC		36	36										
MACHXO		40	40										
XP		38	38										
XP2		36	36										

D7SEGB

7-Segment-Display Decoder for Common-Cathode LED (Active High Output), Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7										
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3			7										
StratixGX		7	7										
Stratix2GX			7										
Max2		7	7										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		8	7										
Spartan2E		8	7										
Spartan3		8	7										
Spartan3A		10	9										
Spartan3ADSP		8	7										
Spartan3AN		8	7										
Spartan3E		8	7										
Spartan3L		8	7										
Virtex		8	7										
Virtex2		8	7										
Virtex2p		8	7										
VirtexE		8	7										
Virtex4		8	7										
Virtex5		8											
CoolRunner2	7												
CoolRunnerXpla3	7												
Xc9500	7												
Xc9500XL	7												
Xc9500XV	7												
ProAsicPlus		29											
ProAsic3		28											
ProAsic3E		28											
Fusion		25											
EC		8	7										
ECP		8	7										
ECP2		8	7										
ECP2M		8	7										
SC		8	7										
MACHXO		8	7										
XP		8	7										
XP2		8	7										

D7SEGNB

7-Segment-Display Decoder for Common-Anode LED (Active Low Output), Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7										
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3			7										
StratixGX		7	7										
Stratix2GX			7										
Max2		7	7										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		8	7										
Spartan2E		8	7										
Spartan3		8	7										
Spartan3A		10	10										
Spartan3ADSP		8	7										
Spartan3AN		10	10										
Spartan3E		8	7										
Spartan3L		8	7										
Virtex		8	7										
Virtex2		8	7										
Virtex2p		8	7										
VirtexE		8	7										
Virtex4		8	7										
Virtex5		8											
CoolRunner2	7												
CoolRunnerXpla3	7												
Xc9500	7												
Xc9500XL	7												
Xc9500XV	7												
ProAsicPlus		28											
ProAsic3		28											
ProAsic3E		26											
Fusion		25											
EC		8	7										
ECP		8	7										
ECP2		8	7										
ECP2M		8	7										
SC		8	7										
MACHXO		10	10										
XP		8	7										
XP2		8	7										

D7SEGNS

7-Segment-Display Decoder for Common-Anode LED (Active Low Output), Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7										
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3			7										
StratixGX		7	7										
Stratix2GX			7										
Max2		7	7										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		8	7										
Spartan2E		8	7										
Spartan3		8	7										
Spartan3A		10	10										
Spartan3ADSP		8	7										
Spartan3AN		10	10										
Spartan3E		8	7										
Spartan3L		8	7										
Virtex		8	7										
Virtex2		8	7										
Virtex2p		8	7										
VirtexE		8	7										
Virtex4		8	7										
Virtex5		8											
CoolRunner2	7												
CoolRunnerXpla3	7												
Xc9500	7												
Xc9500XL	7												
Xc9500XV	7												
ProAsicPlus		29											
ProAsic3		28											
ProAsic3E		26											
Fusion		25											
EC		8	7										
ECP		8	7										
ECP2		8	7										
ECP2M		8	7										
SC		8	7										
MACHXO		10	10										
XP		8	7										
XP2		8	7										

D7SEGS

7-Segment-Display Decoder for Common-Cathode LED (Active High Output), Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7										
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3			7										
StratixGX		7	7										
Stratix2GX			7										
Max2		7	7										
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		8	7										
Spartan2E		8	7										
Spartan3		8	7										
Spartan3A		12	12										
Spartan3ADSP		8	7										
Spartan3AN		12	11										
Spartan3E		8	7										
Spartan3L		8	7										
Virtex		8	7										
Virtex2		8	7										
Virtex2p		8	7										
VirtexE		8	7										
Virtex4		8	7										
Virtex5		8											
CoolRunner2	7												
CoolRunnerXpla3	7												
Xc9500	7												
Xc9500XL	7												
Xc9500XV	7												
ProAsicPlus		29											
ProAsic3		28											
ProAsic3E		28											
Fusion		25											
EC		8	7										
ECP		8	7										
ECP2		8	7										
ECP2M		8	7										
SC		8	7										
MACHXO		10	10										
XP		8	7										
XP2		8	7										

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1