



## FPGA Counter Resource Usage

### Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Counter cores.

Core Reference  
CR0130 (v1.11) December 19, 2008

### Counter

The available Counter cores are listed as follows:

<a href="#">CB2CEB</a>	<a href="#">CB2CES</a>	<a href="#">CB2CLEB</a>	<a href="#">CB2CLEDB</a>
<a href="#">CB2CLEDS</a>	<a href="#">CB2CLES</a>	<a href="#">CB2REB</a>	<a href="#">CB2RES</a>
<a href="#">CB2RLEB</a>	<a href="#">CB2RLES</a>	<a href="#">CB4CEB</a>	<a href="#">CB4CES</a>
<a href="#">CB4CLEB</a>	<a href="#">CB4CLEDB</a>	<a href="#">CB4CLEDS</a>	<a href="#">CB4CLES</a>
<a href="#">CB4REB</a>	<a href="#">CB4RES</a>	<a href="#">CB4RLEB</a>	<a href="#">CB4RLES</a>
<a href="#">CB8CEB</a>	<a href="#">CB8CES</a>	<a href="#">CB8CLEB</a>	<a href="#">CB8CLEDB</a>
<a href="#">CB8CLEDS</a>	<a href="#">CB8CLES</a>	<a href="#">CB8REB</a>	<a href="#">CB8RES</a>
<a href="#">CB8RLEB</a>	<a href="#">CB8RLES</a>	<a href="#">CB16CEB</a>	<a href="#">CB16CES</a>
<a href="#">CB16CLEB</a>	<a href="#">CB16CLEDB</a>	<a href="#">CB16CLEDS</a>	<a href="#">CB16CLES</a>
<a href="#">CB16REB</a>	<a href="#">CB16RES</a>	<a href="#">CB16RLEB</a>	<a href="#">CB16RLES</a>
<a href="#">CB32CEB</a>	<a href="#">CB32CLEB</a>	<a href="#">CB32CLEDB</a>	<a href="#">CB32REB</a>
<a href="#">CB32RLEB</a>	<a href="#">CD4CEB</a>	<a href="#">CD4CES</a>	<a href="#">CD4CLEB</a>
<a href="#">CD4CLES</a>	<a href="#">CD4REB</a>	<a href="#">CD4RES</a>	<a href="#">CD4RLEB</a>
<a href="#">CD4RLES</a>	<a href="#">CJ2CEB</a>	<a href="#">CJ2CES</a>	<a href="#">CJ2REB</a>
<a href="#">CJ2RES</a>	<a href="#">CJ4CEB</a>	<a href="#">CJ4CES</a>	<a href="#">CJ4REB</a>
<a href="#">CJ4RES</a>	<a href="#">CJ5CEB</a>	<a href="#">CJ5CES</a>	<a href="#">CJ5REB</a>
<a href="#">CJ5RES</a>	<a href="#">CJ8CEB</a>	<a href="#">CJ8CES</a>	<a href="#">CJ8REB</a>
<a href="#">CJ8RES</a>	<a href="#">CJ16CEB</a>	<a href="#">CJ16CES</a>	<a href="#">CJ16REB</a>
<a href="#">CJ16RES</a>	<a href="#">CJ32CEB</a>	<a href="#">CJ32REB</a>	<a href="#">CR2CEB</a>
<a href="#">CR2CES</a>	<a href="#">CR4CEB</a>	<a href="#">CR4CES</a>	<a href="#">CR8CEB</a>
<a href="#">CR8CES</a>	<a href="#">CR16CEB</a>	<a href="#">CR16CES</a>	<a href="#">CR32CEB</a>

**FPGA Counter Resource Usage**

**CB2CEB**

**2-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		4	4	2								2	
Cyclone2		4	4	2									
Cyclone3		4	4	2									
Stratix		4	4	2								2	
Stratix2		4	4	2									
Stratix3			4	2								2	
StratixGX		4	4	2								2	
Stratix2GX			4	2								2	
Max2		4	4	2								2	
Max3000a	4	4		2									
Max7000b	4	4		2									
Max7000ae	4	4		2									
Max7000s	4	4		2									
Spartan2		4	4	2									
Spartan2E		4	4	2									
Spartan3		4	4	2									
Spartan3A		6	6	2									
Spartan3ADSP		6	6	2									
Spartan3AN		6	6	2									
Spartan3E		6	6	2									
Spartan3L		6	6	2									
Virtex		4	4	2									
Virtex2		4	4	2									
Virtex2p		4	4	2									
VirtexE		4	4	2									
Virtex4		6	6	2									
Virtex5		4	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		7											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		6	4	2									
ECP		6	4	2									
ECP2		6	4	2									
ECP2M		6	4	2									
SC		4	4	2									
MACHXO		6	4										
XP		6	4	2									
XP2		6	4	2									

## CB2CES

### 2-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		4	4	2								2	
Cyclone2		4	4	2									
Cyclone3		4	4	2									
Stratix		4	4	2								2	
Stratix2		4	4	2									
Stratix3			4	2								2	
StratixGX		4	4	2								2	
Stratix2GX			4	2								2	
Max2		4	4	2								2	
Max3000a	4	4		2									
Max7000b	4	4		2									
Max7000ae	4	4		2									
Max7000s	4	4		2									
Spartan2		4	4	2									
Spartan2E		4	4	2									
Spartan3		4	4	2									
Spartan3A		6	6	2									
Spartan3ADSP		6	6	2									
Spartan3AN		6	6	2									
Spartan3E		6	6	2									
Spartan3L		6	6	2									
Virtex		4	4	2									
Virtex2		4	4	2									
Virtex2p		4	4	2									
VirtexE		4	4	2									
Virtex4		6	6	2									
Virtex5		6	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		7											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		6	4	2									
ECP		6	4	2									
ECP2		6	4	2									
ECP2M		6	4	2									
SC		4	4	2									
MACHXO		6	4										
XP		6	4	2									
XP2		6	4	2									

**FPGA Counter Resource Usage**

**CB2CLEB**

**2-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		5	5	2								2	
Cyclone2		5	5	2									
Cyclone3		5	5	2									
Stratix		5	5	2								2	
Stratix2		4	4	2									
Stratix3			4	2								2	
StratixGX		5	5	2								2	
Stratix2GX			4	2								2	
Max2		5	5	2								2	
Max3000a	4	4		2									
Max7000b	4	4		2									
Max7000ae	4	4		2									
Max7000s	4	4		2									
Spartan2		6	5	2									
Spartan2E		6	5	2									
Spartan3		6	5	2									
Spartan3A		8	7	2									
Spartan3ADSP		8	7	2									
Spartan3AN		8	7	2									
Spartan3E		8	7	2									
Spartan3L		8	7	2									
Virtex		6	5	2									
Virtex2		6	5	2									
Virtex2p		6	5	2									
VirtexE		6	5	2									
Virtex4		8	7	2									
Virtex5		4	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		9											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		6	5	2									
ECP		6	5	2									
ECP2		8	5	2									
ECP2M		8	5	2									
SC		6	5	2									
MACHXO		8	5										
XP		8	5	2									
XP2		8	5	2									

**CB2CLEDB**

**2-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		5	5	2								2	
Cyclone2		5	5	2									
Cyclone3		5	5	2									
Stratix		5	5	2									2
Stratix2		5	5	2									
Stratix3			4	2									2
StratixGX		5	5	2									2
Stratix2GX			4	2									2
Max2		5	5	2									2
Max3000a	4	4		2									
Max7000b	4	4		2									
Max7000ae	4	4		2									
Max7000s	4	4		2									
Spartan2		6	5	2									
Spartan2E		6	5	2									
Spartan3		6	5	2									
Spartan3A		8	7	2									
Spartan3ADSP		8	7	2									
Spartan3AN		8	7	2									
Spartan3E		8	7	2									
Spartan3L		8	7	2									
Virtex		6	5	2									
Virtex2		6	5	2									
Virtex2p		6	5	2									
VirtexE		6	5	2									
Virtex4		8	7	2									
Virtex5		6	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		13											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		6	5	2									
ECP		6	5	2									
ECP2		6	5	2									
ECP2M		6	5	2									
SC		6	5	2									
MACHXO		6	5										
XP		6	5	2									
XP2		6	5	2									

**FPGA Counter Resource Usage**

**CB2CLEDS**

**2-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		5	5	2								2	
Cyclone2		5	5	2									
Cyclone3		5	5	2									
Stratix		5	5	2								2	
Stratix2		5	5	2									
Stratix3			4	2								2	
StratixGX		5	5	2								2	
Stratix2GX			4	2								2	
Max2		5	5	2								2	
Max3000a	4	4		2									
Max7000b	4	4		2									
Max7000ae	4	4		2									
Max7000s	4	4		2									
Spartan2		6	5	2									
Spartan2E		6	5	2									
Spartan3		6	5	2									
Spartan3A		8	7	2									
Spartan3ADSP		8	7	2									
Spartan3AN		8	7	2									
Spartan3E		8	7	2									
Spartan3L		8	7	2									
Virtex		6	5	2									
Virtex2		6	5	2									
Virtex2p		6	5	2									
VirtexE		6	5	2									
Virtex4		8	7	2									
Virtex5		4	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		13											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		6	5	2									
ECP		6	5	2									
ECP2		6	5	2									
ECP2M		6	5	2									
SC		6	5	2									
MACHXO		6	5										
XP		6	5	2									
XP2		6	5	2									

## CB2CLES

### 2-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		5	5	2								2	
Cyclone2		5	5	2									
Cyclone3		5	5	2									
Stratix		5	5	2								2	
Stratix2		4	4	2									
Stratix3			4	2								2	
StratixGX		5	5	2								2	
Stratix2GX			4	2								2	
Max2		5	5	2								2	
Max3000a	4	4		2									
Max7000b	4	4		2									
Max7000ae	4	4		2									
Max7000s	4	4		2									
Spartan2		6	5	2									
Spartan2E		6	5	2									
Spartan3		6	5	2									
Spartan3A		8	7	2									
Spartan3ADSP		8	7	2									
Spartan3AN		8	7	2									
Spartan3E		8	7	2									
Spartan3L		8	7	2									
Virtex		6	5	2									
Virtex2		6	5	2									
Virtex2p		6	5	2									
VirtexE		6	5	2									
Virtex4		8	7	2									
Virtex5		6	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		9											
ProAsic3		8											
ProAsic3E		8											
Fusion		8											
EC		6	5	2									
ECP		6	5	2									
ECP2		8	5	2									
ECP2M		8	5	2									
SC		6	5	2									
MACHXO		8	5										
XP		8	5	2									
XP2		8	5	2									

**FPGA Counter Resource Usage**

**CB2REB**

**2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		4	4	2									1
Cyclone2		4	4	2									
Cyclone3		4	4	2									
Stratix		4	4	2									1
Stratix2		4	4	2									
Stratix3			4	2									1
StratixGX		4	4	2									1
Stratix2GX			4	2									1
Max2		4	4	2									1
Max3000a	4	4		2									
Max7000b	4	4		2									
Max7000ae	4	4		2									
Max7000s	4	4		2									
Spartan2		4	4	2									
Spartan2E		4	4	2									
Spartan3		4	4	2									
Spartan3A		6	6	2									
Spartan3ADSP		6	6	2									
Spartan3AN		6	6	2									
Spartan3E		6	6	2									
Spartan3L		6	6	2									
Virtex		4	4	2									
Virtex2		4	4	2									
Virtex2p		4	4	2									
VirtexE		4	4	2									
Virtex4		6	6	2									
Virtex5		4	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		9											
ProAsic3		7											
ProAsic3E		7											
Fusion		7											
EC		6	4	2									
ECP		6	4	2									
ECP2		6	4	2									
ECP2M		6	4	2									
SC		4	4	2									
MACHXO		6	4										
XP		6	4	2									
XP2		6	4	2									



## CB2RES

### 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		4	4	2									1
Cyclone2		4	4	2									
Cyclone3		4	4	2									
Stratix		4	4	2									1
Stratix2		4	4	2									
Stratix3			4	2									1
StratixGX		4	4	2									1
Stratix2GX			4	2									1
Max2		4	4	2									1
Max3000a	4	4		2									
Max7000b	4	4		2									
Max7000ae	4	4		2									
Max7000s	4	4		2									
Spartan2		4	4	2									
Spartan2E		4	4	2									
Spartan3		4	4	2									
Spartan3A		6	6	2									
Spartan3ADSP		6	6	2									
Spartan3AN		6	6	2									
Spartan3E		6	6	2									
Spartan3L		6	6	2									
Virtex		4	4	2									
Virtex2		4	4	2									
Virtex2p		4	4	2									
VirtexE		4	4	2									
Virtex4		6	6	2									
Virtex5		6	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		9											
ProAsic3		7											
ProAsic3E		7											
Fusion		7											
EC		6	4	2									
ECP		6	4	2									
ECP2		6	4	2									
ECP2M		6	4	2									
SC		4	4	2									
MACHXO		6	4										
XP		6	4	2									
XP2		6	4	2									

**FPGA Counter Resource Usage**

**CB2RLEB**

**2-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		6	6	2									1
Cyclone2		6	6	2									
Cyclone3		6	6	2									
Stratix		6	6	2									1
Stratix2		5	5	2									
Stratix3			4	2									1
StratixGX		6	6	2									1
Stratix2GX			4	2									1
Max2		6	6	2									1
Max3000a	4	4		2									
Max7000b	4	4		2									
Max7000ae	4	4		2									
Max7000s	4	4		2									
Spartan2		6	5	2									
Spartan2E		6	5	2									
Spartan3		6	5	2									
Spartan3A		8	7	2									
Spartan3ADSP		8	7	2									
Spartan3AN		8	7	2									
Spartan3E		8	7	2									
Spartan3L		8	7	2									
Virtex		6	5	2									
Virtex2		6	5	2									
Virtex2p		6	5	2									
VirtexE		6	5	2									
Virtex4		8	7	2									
Virtex5		6	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		11											
ProAsic3		10											
ProAsic3E		10											
Fusion		10											
EC		8	6	2									
ECP		8	6	2									
ECP2		8	5	2									
ECP2M		8	5	2									
SC		6	5	2									
MACHXO		8	7										
XP		8	7	2									
XP2		8	5	2									

## CB2RLES

### 2-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	2									
Cyclone		6	6	2									1
Cyclone2		6	6	2									
Cyclone3		6	6	2									
Stratix		6	6	2									1
Stratix2		5	5	2									
Stratix3			4	2									1
StratixGX		6	6	2									1
Stratix2GX			4	2									1
Max2		6	6	2									1
Max3000a	4	4		2									
Max7000b	4	4		2									
Max7000ae	4	4		2									
Max7000s	4	4		2									
Spartan2		6	5	2									
Spartan2E		6	5	2									
Spartan3		6	5	2									
Spartan3A		8	7	2									
Spartan3ADSP		8	7	2									
Spartan3AN		8	7	2									
Spartan3E		8	7	2									
Spartan3L		8	7	2									
Virtex		6	5	2									
Virtex2		6	5	2									
Virtex2p		6	5	2									
VirtexE		6	5	2									
Virtex4		8	7	2									
Virtex5		6	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		11											
ProAsic3		10											
ProAsic3E		10											
Fusion		10											
EC		8	6	2									
ECP		8	6	2									
ECP2		8	5	2									
ECP2M		8	5	2									
SC		6	5	2									
MACHXO		8	7										
XP		8	7	2									
XP2		8	5	2									

**FPGA Counter Resource Usage**

**CB4CEB**

**4-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6	4									
Cyclone		6	6	4							2	
Cyclone2		6	6	4								
Cyclone3		6	6	4								
Stratix		6	6	4							2	
Stratix2		6	6	4								
Stratix3			6	4							2	
StratixGX		6	6	4							2	
Stratix2GX			6	4							2	
Max2		7	7	4							2	
Max3000a	6	6		4								
Max7000b	6	6		4								
Max7000ae	6	6		4								
Max7000s	6	6		4								
Spartan2		8	7	4								
Spartan2E		8	7	4								
Spartan3		8	7	4								
Spartan3A		12	10	4								
Spartan3ADSP		12	11	4								
Spartan3AN		12	10	4								
Spartan3E		12	11	4								
Spartan3L		12	11	4								
Virtex		8	7	4								
Virtex2		8	7	4								
Virtex2p		8	7	4								
VirtexE		8	7	4								
Virtex4		12	11	4								
Virtex5		6	4	4								
CoolRunner2	6			4								
CoolRunnerXpla3	6			4								
Xc9500	6			4								
Xc9500XL	6			4								
Xc9500XV	6			4								
ProAsicPlus		14										
ProAsic3		13										
ProAsic3E		13										
Fusion		13										
EC		6	6	4								
ECP		6	6	4								
ECP2		10	6	4								
ECP2M		10	6	4								
SC		10	6	4								
MACHXO		10	6									
XP		10	6	4								
XP2		10	6	4								

## CB4CES

### 4-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	4									
Cyclone		6	6	4								2	
Cyclone2		6	6	4									
Cyclone3		6	6	4									
Stratix		6	6	4								2	
Stratix2		6	6	4									
Stratix3			6	4								2	
StratixGX		6	6	4								2	
Stratix2GX			6	4								2	
Max2		7	7	4								2	
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		8	7	4									
Spartan2E		8	7	4									
Spartan3		8	7	4									
Spartan3A													
Spartan3ADSP		12	11	4									
Spartan3AN		12	11	4									
Spartan3E		12	11	4									
Spartan3L		12	11	4									
Virtex		8	7	4									
Virtex2		8	7	4									
Virtex2p		8	7	4									
VirtexE		8	7	4									
Virtex4		12	11	4									
Virtex5		6	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		14											
ProAsic3		13											
ProAsic3E		13											
Fusion		13											
EC		6	6	4									
ECP		6	6	4									
ECP2		10	6	4									
ECP2M		10	6	4									
SC		10	6	4									
MACHXO		10	6										
XP		10	6	4									
XP2		10	6	4									

**FPGA Counter Resource Usage**

**CB4CLEB**

**4-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	4									
Cyclone		6	6	4								2	
Cyclone2		7	7	4									
Cyclone3		6	6	4									
Stratix		6	6	4								2	
Stratix2		7	7	4									
Stratix3			6	4								2	
StratixGX		6	6	4								2	
Stratix2GX			6	4								2	
Max2		9	9	4								2	
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		10	9	4									
Spartan2E		10	9	4									
Spartan3		10	9	4									
Spartan3A													
Spartan3ADSP		14	13	4									
Spartan3AN		14	13	4									
Spartan3E		14	13	4									
Spartan3L		14	13	4									
Virtex		10	9	4									
Virtex2		10	9	4									
Virtex2p		10	9	4									
VirtexE		10	9	4									
Virtex4		14	13	4									
Virtex5		6	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		18											
ProAsic3		17											
ProAsic3E		17											
Fusion		17											
EC		12	11	4									
ECP		12	11	4									
ECP2		12	9	4									
ECP2M		12	9	4									
SC		12	9	4									
MACHXO		12	9										
XP		14	9	4									
XP2		12	9	4									

## CB4CLEDB

### 4-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	4									
Cyclone		10	10	4								2	
Cyclone2		10	10	4									
Cyclone3		12	12	4									
Stratix		10	10	4								2	
Stratix2		10	10	4									
Stratix3			7	4								2	
StratixGX		10	10	4								2	
Stratix2GX			7	4								2	
Max2		11	11	4								2	
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		12	10	4									
Spartan2E		12	10	4									
Spartan3		14	12	4									
Spartan3A		18	18	4									
Spartan3ADSP		18	17	4									
Spartan3AN		18	18	4									
Spartan3E		18	17	4									
Spartan3L		18	17	4									
Virtex		12	10	4									
Virtex2		14	13	4									
Virtex2p		14	13	4									
VirtexE		12	10	4									
Virtex4		18	16	4									
Virtex5		10	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		29											
ProAsic3		28											
ProAsic3E		26											
Fusion		24											
EC		20	17	4									
ECP		20	17	4									
ECP2		28	18	4									
ECP2M		28	18	4									
SC		14	12	4									
MACHXO		22	14										
XP		16	13	4									
XP2		20	14	4									

**FPGA Counter Resource Usage**

**CB4CLEDS**

**4-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	4									
Cyclone		10	10	4								2	
Cyclone2		10	10	4									
Cyclone3		12	12	4									
Stratix		10	10	4								2	
Stratix2		10	10	4									
Stratix3			7	4								2	
StratixGX		10	10	4								2	
Stratix2GX			7	4								2	
Max2		11	11	4								2	
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		12	10	4									
Spartan2E		12	10	4									
Spartan3		14	12	4									
Spartan3A		18	18	4									
Spartan3ADSP		18	17	4									
Spartan3AN		18	18	4									
Spartan3E		18	17	4									
Spartan3L		18	17	4									
Virtex		12	10	4									
Virtex2		14	13	4									
Virtex2p		14	13	4									
VirtexE		12	10	4									
Virtex4		18	16	4									
Virtex5		8	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		29											
ProAsic3		28											
ProAsic3E		26											
Fusion		24											
EC		20	17	4									
ECP		20	17	4									
ECP2		28	18	4									
ECP2M		28	18	4									
SC		14	12	4									
MACHXO		22	14										
XP		16	13	4									
XP2		20	14	4									



## CB4CLES

### 4-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	4									
Cyclone		6	6	4								2	
Cyclone2		7	7	4									
Cyclone3		6	6	4									
Stratix		6	6	4								2	
Stratix2		7	7	4									
Stratix3			6	4								2	
StratixGX		6	6	4								2	
Stratix2GX			6	4								2	
Max2		9	9	4								2	
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		10	9	4									
Spartan2E		10	9	4									
Spartan3		10	9	4									
Spartan3A		14	13	4									
Spartan3ADSP		14	13	4									
Spartan3AN		14	13	4									
Spartan3E		14	13	4									
Spartan3L		14	13	4									
Virtex		10	9	4									
Virtex2		10	9	4									
Virtex2p		10	9	4									
VirtexE		10	9	4									
Virtex4		14	13	4									
Virtex5		8	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		18											
ProAsic3		17											
ProAsic3E		17											
Fusion		17											
EC		12	11	4									
ECP		12	11	4									
ECP2		12	9	4									
ECP2M		12	9	4									
SC		12	9	4									
MACHXO		12	9										
XP		14	9	4									
XP2		12	9	4									

**FPGA Counter Resource Usage**

**CB4REB**

**4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	4									
Cyclone		7	6	4									1
Cyclone2		7	7	4									
Cyclone3		7	7	4									
Stratix		7	6	4									1
Stratix2		7	7	4									
Stratix3			7	4									1
StratixGX		7	7	4									1
Stratix2GX			6	4									1
Max2		7	7	4									1
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		8	7	4									
Spartan2E		8	7	4									
Spartan3		8	7	4									
Spartan3A		12	10	4									
Spartan3ADSP		12	11	4									
Spartan3AN		12	10	4									
Spartan3E		12	11	4									
Spartan3L		12	11	4									
Virtex		8	7	4									
Virtex2		8	7	4									
Virtex2p		8	7	4									
VirtexE		8	7	4									
Virtex4		12	11	4									
Virtex5		6	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		18											
ProAsic3		14											
ProAsic3E		14											
Fusion		14											
EC		16	11	4									
ECP		16	11	4									
ECP2		12	7	4									
ECP2M		12	7	4									
SC		12	7	4									
MACHXO		12	9										
XP		10	8	4									
XP2		12	7	4									

## CB4RES

### 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	4									
Cyclone		7	6	4									1
Cyclone2		7	7	4									
Cyclone3		7	7	4									
Stratix		7	6	4									1
Stratix2		7	7	4									
Stratix3			7	4									1
StratixGX		7	7	4									1
Stratix2GX			6	4									1
Max2		7	7	4									1
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		8	7	4									
Spartan2E		8	7	4									
Spartan3		8	7	4									
Spartan3A		12	10	4									
Spartan3ADSP		12	11	4									
Spartan3AN		12	10	4									
Spartan3E		12	11	4									
Spartan3L		12	11	4									
Virtex		8	7	4									
Virtex2		8	7	4									
Virtex2p		8	7	4									
VirtexE		8	7	4									
Virtex4		12	11	4									
Virtex5		6	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		18											
ProAsic3		14											
ProAsic3E		14											
Fusion		14											
EC		16	11	4									
ECP		16	11	4									
ECP2		12	7	4									
ECP2M		12	7	4									
SC		12	7	4									
MACHXO		12	9										
XP		10	8	4									
XP2		12	7	4									

FPGA Counter Resource Usage

**CB4RLEB**

**4-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	4									
Cyclone		11	11	4									1
Cyclone2		7	7	4									
Cyclone3		6	6	4									
Stratix		11	11	4									1
Stratix2		8	8	4									
Stratix3			6	4									1
StratixGX		11	11	4									1
Stratix2GX			11	4									1
Max2		11	11	4									1
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		10	9	4									
Spartan2E		10	9	4									
Spartan3		10	9	4									
Spartan3A		14	13	4									
Spartan3ADSP		14	13	4									
Spartan3AN		14	13	4									
Spartan3E		14	13	4									
Spartan3L		14	13	4									
Virtex		10	9	4									
Virtex2		10	9	4									
Virtex2p		10	9	4									
VirtexE		10	9	4									
Virtex4		14	13	4									
Virtex5		6	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		22											
ProAsic3		21											
ProAsic3E		21											
Fusion		21											
EC		16	11	4									
ECP		16	11	4									
ECP2		12	10	4									
ECP2M		12	10	4									
SC		12	10	4									
MACHXO		12	11										
XP		12	10	4									
XP2		12	11	4									

## CB4RLES

### 4-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	4									
Cyclone		11	11	4									1
Cyclone2		7	7	4									
Cyclone3		6	6	4									
Stratix		11	11	4									1
Stratix2		8	8	4									
Stratix3			6	4									1
StratixGX		11	11	4									1
Stratix2GX			11	4									1
Max2		11	11	4									1
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		10	9	4									
Spartan2E		10	9	4									
Spartan3		10	9	4									
Spartan3A		14	13	4									
Spartan3ADSP		14	13	4									
Spartan3AN		14	13	4									
Spartan3E		14	13	4									
Spartan3L		14	13	4									
Virtex		10	9	4									
Virtex2		10	9	4									
Virtex2p		10	9	4									
VirtexE		10	9	4									
Virtex4		14	13	4									
Virtex5		6	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		22											
ProAsic3		21											
ProAsic3E		21											
Fusion		21											
EC		16	11	4									
ECP		16	11	4									
ECP2		12	10	4									
ECP2M		12	10	4									
SC		12	10	4									
MACHXO		12	11										
XP		12	10	4									
XP2		12	11	4									

**FPGA Counter Resource Usage**

**CB8CEB**

**8-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			11	8									
Cyclone		12	12	8								2	
Cyclone2		12	12	8									
Cyclone3		12	12	8									
Stratix		12	12	8								2	
Stratix2		12	12	8									
Stratix3			11	8								2	
StratixGX		12	12	8								2	
Stratix2GX			11	8								2	
Max2		12	12	8								2	
Max3000a	10	10		8									
Max7000b	10	10		8									
Max7000ae	10	10		8									
Max7000s	10	10		8									
Spartan2		12	4	8									
Spartan2E		12	4	8									
Spartan3		12	4	8									
Spartan3A		22	12	8									
Spartan3ADSP		22	12	8									
Spartan3AN		22	12	8									
Spartan3E		22	12	8									
Spartan3L		22	12	8									
Virtex		12	4	8									
Virtex2		12	4	8									
Virtex2p		12	4	8									
VirtexE		12	4	8									
Virtex4		20	12	8									
Virtex5		10	9	9									
CoolRunner2	10			8									
CoolRunnerXpla3	10			8									
Xc9500	10			8									
Xc9500XL	10			8									
Xc9500XV	10			8									
ProAsicPlus		30											
ProAsic3		25											
ProAsic3E		25											
Fusion		25											
EC		12	12	8									
ECP		12	12	8									
ECP2		18	16	8									
ECP2M		18	16	8									
SC		12	12	8									
MACHXO		12	12										
XP		12	12	8									
XP2		16	15	8									

## CB8CES

### 8-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			11	8									
Cyclone		12	12	8								2	
Cyclone2		12	12	8									
Cyclone3		12	12	8									
Stratix		12	12	8								2	
Stratix2		12	12	8									
Stratix3			11	8								2	
StratixGX		12	12	8								2	
Stratix2GX			11	8								2	
Max2		12	12	8								2	
Max3000a	10	10		8									
Max7000b	10	10		8									
Max7000ae	10	10		8									
Max7000s	10	10		8									
Spartan2		12	4	8									
Spartan2E		12	4	8									
Spartan3		12	4	8									
Spartan3A		22	12	8									
Spartan3ADSP		22	12	8									
Spartan3AN		22	12	8									
Spartan3E		22	12	8									
Spartan3L		22	12	8									
Virtex		12	4	8									
Virtex2		12	4	8									
Virtex2p		12	4	8									
VirtexE		12	4	8									
Virtex4		20	12	8									
Virtex5		8	9	9									
CoolRunner2	10			8									
CoolRunnerXpla3	10			8									
Xc9500	10			8									
Xc9500XL	10			8									
Xc9500XV	10			8									
ProAsicPlus		30											
ProAsic3		25											
ProAsic3E		25											
Fusion		25											
EC		12	12	8									
ECP		12	12	8									
ECP2		18	16	8									
ECP2M		18	16	8									
SC		12	12	8									
MACHXO		12	12										
XP		12	12	8									
XP2		16	15	8									

**FPGA Counter Resource Usage**

**CB8CLEB**

**8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			11	8									
Cyclone		12	12	8								2	
Cyclone2		13	13	8									
Cyclone3		13	13	8									
Stratix		12	12	8								2	
Stratix2		12	12	8									
Stratix3			11	8								2	
StratixGX		12	12	8								2	
Stratix2GX			11	8								2	
Max2		12	12	8								2	
Max3000a	10	10		8									
Max7000b	10	10		8									
Max7000ae	10	10		8									
Max7000s	10	10		8									
Spartan2		14	13	8									
Spartan2E		14	13	8									
Spartan3		14	13	8									
Spartan3A		22	21	8									
Spartan3ADSP		22	21	8									
Spartan3AN		22	21	8									
Spartan3E		22	21	8									
Spartan3L		22	21	8									
Virtex		14	13	8									
Virtex2		14	13	8									
Virtex2p		14	13	8									
VirtexE		14	13	8									
Virtex4		22	21	8									
Virtex5		8	8	8									
CoolRunner2	10			8									
CoolRunnerXpla3	10			8									
Xc9500	10			8									
Xc9500XL	10			8									
Xc9500XV	10			8									
ProAsicPlus		38											
ProAsic3		33											
ProAsic3E		33											
Fusion		33											
EC		26	25	8									
ECP		26	25	8									
ECP2		20	17	8									
ECP2M		20	17	8									
SC		30	21	8									
MACHXO		16	14										
XP		30	21	8									
XP2		18	16	8									



## CB8CLEDB

### 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			15	8									
Cyclone		17	17	8								2	
Cyclone2		17	17	8									
Cyclone3		29	29	8									
Stratix		17	17	8								2	
Stratix2		13	13	8									
Stratix3			15	8								2	
StratixGX		17	17	8								2	
Stratix2GX			13	8								2	
Max2		17	17	8								2	
Max3000a	11	11		8									
Max7000b	11	11		8									
Max7000ae	11	11		8									
Max7000s	11	11		8									
Spartan2		18	16	8									
Spartan2E		18	16	8									
Spartan3		20	17	8									
Spartan3A		26	25	8									
Spartan3ADSP		26	25	8									
Spartan3AN		26	25	8									
Spartan3E		26	25	8									
Spartan3L		26	25	8									
Virtex		18	16	8									
Virtex2		20	17	8									
Virtex2p		20	17	8									
VirtexE		18	16	8									
Virtex4		26	25	8									
Virtex5		12	8	8									
CoolRunner2	10			8									
CoolRunnerXpla3	10			8									
Xc9500	10			8									
Xc9500XL	10			8									
Xc9500XV	10			8									
ProAsicPlus		66											
ProAsic3		61											
ProAsic3E		56											
Fusion		53											
EC		34	33	8									
ECP		34	33	8									
ECP2		30	28	8									
ECP2M		30	28	8									
SC		34	24	8									
MACHXO		26	26										
XP		40	27	8									
XP2		30	28	8									

**FPGA Counter Resource Usage**

**CB8CLEDS**

**8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			15	8									
Cyclone		17	17	8								2	
Cyclone2		17	17	8									
Cyclone3		29	29	8									
Stratix		17	17	8								2	
Stratix2		13	13	8									
Stratix3			15	8								2	
StratixGX		17	17	8								2	
Stratix2GX			13	8								2	
Max2		17	17	8								2	
Max3000a	11	11		8									
Max7000b	11	11		8									
Max7000ae	11	11		8									
Max7000s	11	11		8									
Spartan2		18	16	8									
Spartan2E		18	16	8									
Spartan3		20	17	8									
Spartan3A		26	25	8									
Spartan3ADSP		26	25	8									
Spartan3AN		26	25	8									
Spartan3E		26	25	8									
Spartan3L		26	25	8									
Virtex		18	16	8									
Virtex2		20	17	8									
Virtex2p		20	17	8									
VirtexE		18	16	8									
Virtex4		26	25	8									
Virtex5		10	8	8									
CoolRunner2	10			8									
CoolRunnerXpla3	10			8									
Xc9500	10			8									
Xc9500XL	10			8									
Xc9500XV	10			8									
ProAsicPlus		66											
ProAsic3		61											
ProAsic3E		56											
Fusion		53											
EC		34	33	8									
ECP		34	33	8									
ECP2		30	28	8									
ECP2M		30	28	8									
SC		34	24	8									
MACHXO		26	26										
XP		40	27	8									
XP2		30	28	8									

## CB8CLES

### 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			11	8									
Cyclone		12	12	8								2	
Cyclone2		13	13	8									
Cyclone3		13	13	8									
Stratix		12	12	8								2	
Stratix2		12	12	8									
Stratix3			11	8								2	
StratixGX		12	12	8								2	
Stratix2GX			11	8								2	
Max2		12	12	8								2	
Max3000a	10	10		8									
Max7000b	10	10		8									
Max7000ae	10	10		8									
Max7000s	10	10		8									
Spartan2		14	13	8									
Spartan2E		14	13	8									
Spartan3		14	13	8									
Spartan3A		22	21	8									
Spartan3ADSP		22	21	8									
Spartan3AN		22	21	8									
Spartan3E		22	21	8									
Spartan3L		22	21	8									
Virtex		14	13	8									
Virtex2		14	13	8									
Virtex2p		14	13	8									
VirtexE		14	13	8									
Virtex4		22	21	8									
Virtex5		8	8	8									
CoolRunner2	10			8									
CoolRunnerXpla3	10			8									
Xc9500	10			8									
Xc9500XL	10			8									
Xc9500XV	10			8									
ProAsicPlus		38											
ProAsic3		33											
ProAsic3E		33											
Fusion		33											
EC		26	25	8									
ECP		26	25	8									
ECP2		20	17	8									
ECP2M		20	17	8									
SC		30	21	8									
MACHXO		16	14										
XP		30	21	8									
XP2		18	16	8									

**FPGA Counter Resource Usage**

**CB8REB**

**8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			12	8									
Cyclone		13	12	8									1
Cyclone2		13	13	8									
Cyclone3		14	14	8									
Stratix		13	12	8									1
Stratix2		12	12	8									
Stratix3			12	8									1
StratixGX		13	13	8									1
Stratix2GX			11	8									1
Max2		13	12	8									1
Max3000a	10	10		8									
Max7000b	10	10		8									
Max7000ae	10	10		8									
Max7000s	10	10		8									
Spartan2		12	4	8									
Spartan2E		12	4	8									
Spartan3		12	4	8									
Spartan3A		22	12	8									
Spartan3ADSP		22	12	8									
Spartan3AN		22	12	8									
Spartan3E		22	12	8									
Spartan3L		22	12	8									
Virtex		12	4	8									
Virtex2		12	4	8									
Virtex2p		12	4	8									
VirtexE		12	4	8									
Virtex4		20	12	8									
Virtex5		10	9	9									
CoolRunner2	10			8									
CoolRunnerXpla3	10			8									
Xc9500	10			8									
Xc9500XL	10			8									
Xc9500XV	10			8									
ProAsicPlus		38											
ProAsic3		28											
ProAsic3E		28											
Fusion		28											
EC		30	21	8									
ECP		30	21	8									
ECP2		20	17	8									
ECP2M		20	17	8									
SC		16	14	8									
MACHXO		16	14										
XP		18	15	8									
XP2		18	16	8									

## CB8RES

### 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			12	8									
Cyclone		13	12	8									1
Cyclone2		13	13	8									
Cyclone3		14	14	8									
Stratix		13	12	8									1
Stratix2		12	12	8									
Stratix3			12	8									1
StratixGX		13	13	8									1
Stratix2GX			11	8									1
Max2		13	12	8									1
Max3000a	11	11		8									
Max7000b	11	11		8									
Max7000ae	11	11		8									
Max7000s	11	11		8									
Spartan2		12	4	8									
Spartan2E		12	4	8									
Spartan3		12	4	8									
Spartan3A		22	12	8									
Spartan3ADSP		22	12	8									
Spartan3AN		22	12	8									
Spartan3E		22	12	8									
Spartan3L		22	12	8									
Virtex		12	4	8									
Virtex2		12	4	8									
Virtex2p		12	4	8									
VirtexE		12	4	8									
Virtex4		20	12	8									
Virtex5		8	9	9									
CoolRunner2	10			8									
CoolRunnerXpla3	10			8									
Xc9500	10			8									
Xc9500XL	10			8									
Xc9500XV	10			8									
ProAsicPlus		38											
ProAsic3		28											
ProAsic3E		28											
Fusion		28											
EC		30	21	8									
ECP		30	21	8									
ECP2		20	17	8									
ECP2M		20	17	8									
SC		16	14	8									
MACHXO		16	14										
XP		18	15	8									
XP2		18	16	8									

**FPGA Counter Resource Usage**

**CB8RLEB**

**8-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			11	8									
Cyclone		21	21	8									1
Cyclone2		13	13	8									
Cyclone3		13	13	8									
Stratix		21	21	8									1
Stratix2		12	12	8									
Stratix3			11	8									1
StratixGX		21	21	8									1
Stratix2GX			20	8									1
Max2		12	12	8									1
Max3000a	11	11		8									
Max7000b	11	11		8									
Max7000ae	11	11		8									
Max7000s	11	11		8									
Spartan2		14	13	8									
Spartan2E		14	13	8									
Spartan3		14	13	8									
Spartan3A		22	21	8									
Spartan3ADSP		22	21	8									
Spartan3AN		22	21	8									
Spartan3E		22	21	8									
Spartan3L		22	21	8									
Virtex		14	13	8									
Virtex2		14	13	8									
Virtex2p		14	13	8									
VirtexE		14	13	8									
Virtex4		22	21	8									
Virtex5		8	8	8									
CoolRunner2	10			8									
CoolRunnerXpla3	10			8									
Xc9500	10			8									
Xc9500XL	10			8									
Xc9500XV	10			8									
ProAsicPlus		46											
ProAsic3		41											
ProAsic3E		41											
Fusion		41											
EC		30	21	8									
ECP		30	21	8									
ECP2		38	26	8									
ECP2M		38	26	8									
SC		32	23	8									
MACHXO		32	22										
XP		36	24	8									
XP2		36	25	8									

## CB8RLES

### 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			11	8									
Cyclone		21	21	8									1
Cyclone2		13	13	8									
Cyclone3		13	13	8									
Stratix		21	21	8									1
Stratix2		12	12	8									
Stratix3			11	8									1
StratixGX		21	21	8									1
Stratix2GX			20	8									1
Max2		12	12	8									1
Max3000a	11	11		8									
Max7000b	11	11		8									
Max7000ae	11	11		8									
Max7000s	11	11		8									
Spartan2		14	13	8									
Spartan2E		14	13	8									
Spartan3		14	13	8									
Spartan3A		22	21	8									
Spartan3ADSP		22	21	8									
Spartan3AN		22	21	8									
Spartan3E		22	21	8									
Spartan3L		22	21	8									
Virtex		14	13	8									
Virtex2		14	13	8									
Virtex2p		14	13	8									
VirtexE		14	13	8									
Virtex4		22	21	8									
Virtex5		8	8	8									
CoolRunner2	10			8									
CoolRunnerXpla3	10			8									
Xc9500	10			8									
Xc9500XL	10			8									
Xc9500XV	10			8									
ProAsicPlus		46											
ProAsic3		41											
ProAsic3E		41											
Fusion		41											
EC		30	21	8									
ECP		30	21	8									
ECP2		38	26	8									
ECP2M		38	26	8									
SC		32	23	8									
MACHXO		32	22										
XP		36	24	8									
XP2		36	25	8									

**FPGA Counter Resource Usage**

**CB16CEB**

**16-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear,  
Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			21	16									
Cyclone		22	22	16								2	
Cyclone2		22	22	16									
Cyclone3		22	22	16									
Stratix		22	22	16								2	
Stratix2		22	22	16									
Stratix3			21	16								2	
StratixGX		22	22	16								2	
Stratix2GX			21	16								2	
Max2		22	22	16								2	
Max3000a	18	18		16									
Max7000b	18	18		16									
Max7000ae	18	18		16									
Max7000s	18	18		16									
Spartan2		22	6	16									
Spartan2E		22	6	16									
Spartan3		22	6	16									
Spartan3A		42	24	16									
Spartan3ADSP		42	24	16									
Spartan3AN		42	24	16									
Spartan3E		40	22	16									
Spartan3L		40	22	16									
Virtex		22	6	16									
Virtex2		22	6	16									
Virtex2p		22	6	16									
VirtexE		22	6	16									
Virtex4		38	22	16									
Virtex5		16	17	17									
CoolRunner2	18			16									
CoolRunnerXpla3	18			16									
Xc9500	18			16									
Xc9500XL	18			16									
Xc9500XV	18			16									
ProAsicPlus		64											
ProAsic3		53											
ProAsic3E		55											
Fusion		53											
EC		24	22	16									
ECP		24	22	16									
ECP2		28	26	16									
ECP2M		28	26	16									
SC		22	22	16									
MACHXO		22	22										
XP		22	22	16									
XP2		26	25	16									



## CB16CES

### 16-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			21	16									
Cyclone		22	22	16								2	
Cyclone2		22	22	16									
Cyclone3		22	22	16									
Stratix		22	22	16								2	
Stratix2		22	22	16									
Stratix3			21	16								2	
StratixGX		22	22	16								2	
Stratix2GX			21	16								2	
Max2		22	22	16								2	
Max3000a	18	18		16									
Max7000b	18	18		16									
Max7000ae	18	18		16									
Max7000s	18	18		16									
Spartan2		22	6	16									
Spartan2E		22	6	16									
Spartan3		22	6	16									
Spartan3A		42	24	16									
Spartan3ADSP		42	24	16									
Spartan3AN		42	24	16									
Spartan3E		40	22	16									
Spartan3L		40	22	16									
Virtex		22	6	16									
Virtex2		22	6	16									
Virtex2p		22	6	16									
VirtexE		22	6	16									
Virtex4		38	22	16									
Virtex5		14	17	17									
CoolRunner2	18			16									
CoolRunnerXpla3	18			16									
Xc9500	18			16									
Xc9500XL	18			16									
Xc9500XV	18			16									
ProAsicPlus		64											
ProAsic3		53											
ProAsic3E		55											
Fusion		53											
EC		24	22	16									
ECP		24	22	16									
ECP2		28	26	16									
ECP2M		28	26	16									
SC		22	22	16									
MACHXO		22	22										
XP		22	22	16									
XP2		26	25	16									

**FPGA Counter Resource Usage**

**CB16CLEB**

**16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			22	16									
Cyclone		23	23	16								2	
Cyclone2		23	23	16									
Cyclone3		23	23	16									
Stratix		23	23	16								2	
Stratix2		23	23	16									
Stratix3			21	16								2	
StratixGX		23	23	16								2	
Stratix2GX			22	16								2	
Max2		23	23	16								2	
Max3000a	18	18		16									
Max7000b	18	18		16									
Max7000ae	18	18		16									
Max7000s	18	18		16									
Spartan2		24	23	16									
Spartan2E		24	23	16									
Spartan3		24	23	16									
Spartan3A		40	39	16									
Spartan3ADSP		40	39	16									
Spartan3AN		40	39	16									
Spartan3E		40	39	16									
Spartan3L		40	39	16									
Virtex		24	23	16									
Virtex2		24	23	16									
Virtex2p		24	23	16									
VirtexE		24	23	16									
Virtex4		40	39	16									
Virtex5		14	16	16									
CoolRunner2	18			16									
CoolRunnerXpla3	18			16									
Xc9500	18			16									
Xc9500XL	18			16									
Xc9500XV	18			16									
ProAsicPlus		80											
ProAsic3		69											
ProAsic3E		72											
Fusion		69											
EC		52	51	16									
ECP		52	51	16									
ECP2		30	27	16									
ECP2M		30	27	16									
SC		56	39	16									
MACHXO		26	24										
XP		56	39	16									
XP2		28	26	16									

## CB16CLEDB

### 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			27	16									
Cyclone		30	30	16								2	
Cyclone2		30	30	16									
Cyclone3		70	70	16									
Stratix		30	30	16								2	
Stratix2		27	27	16									
Stratix3			27	16								2	
StratixGX		30	30	16								2	
Stratix2GX			25	16								2	
Max2		30	30	16								2	
Max3000a	27	27		16									
Max7000b	27	27		16									
Max7000ae	27	27		16									
Max7000s	27	27		16									
Spartan2		32	30	16									
Spartan2E		32	30	16									
Spartan3		34	31	16									
Spartan3A		46	46	16									
Spartan3ADSP		48	47	16									
Spartan3AN		46	46	16									
Spartan3E		46	46	16									
Spartan3L		48	47	16									
Virtex		32	30	16									
Virtex2		34	31	16									
Virtex2p		34	31	16									
VirtexE		32	30	16									
Virtex4		48	47	16									
Virtex5		16	16	16									
CoolRunner2	19			16									
CoolRunnerXpla3	19			16									
Xc9500	18			16									
Xc9500XL	18			16									
Xc9500XV	18			16									
ProAsicPlus		143											
ProAsic3		175											
ProAsic3E		154											
Fusion		110											
EC		62	62	16									
ECP		62	62	16									
ECP2		68	50	16									
ECP2M		68	50	16									
SC		64	46	16									
MACHXO		58	47										
XP		78	52	16									
XP2		66	50	16									

**FPGA Counter Resource Usage**

**CB16CLEDS**

**16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			27	16									
Cyclone		30	30	16								2	
Cyclone2		30	30	16									
Cyclone3		70	70	16									
Stratix		30	30	16								2	
Stratix2		27	27	16									
Stratix3			27	16								2	
StratixGX		30	30	16								2	
Stratix2GX			25	16								2	
Max2		30	30	16								2	
Max3000a	27	27		16									
Max7000b	27	27		16									
Max7000ae	27	27		16									
Max7000s	27	27		16									
Spartan2		32	30	16									
Spartan2E		32	30	16									
Spartan3		34	31	16									
Spartan3A		46	46	16									
Spartan3ADSP		48	47	16									
Spartan3AN		46	46	16									
Spartan3E		46	46	16									
Spartan3L		48	47	16									
Virtex		32	30	16									
Virtex2		34	31	16									
Virtex2p		34	31	16									
VirtexE		32	30	16									
Virtex4		48	47	16									
Virtex5		18	16	16									
CoolRunner2	18			16									
CoolRunnerXpla3	18			16									
Xc9500	18			16									
Xc9500XL	18			16									
Xc9500XV	18			16									
ProAsicPlus		143											
ProAsic3		175											
ProAsic3E		154											
Fusion		110											
EC		62	62	16									
ECP		62	62	16									
ECP2		68	50	16									
ECP2M		68	50	16									
SC		64	46	16									
MACHXO		58	47										
XP		78	52	16									
XP2		66	50	16									

## CB16CLES

### 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			22	16									
Cyclone		23	23	16								2	
Cyclone2		23	23	16									
Cyclone3		23	23	16									
Stratix		23	23	16								2	
Stratix2		23	23	16									
Stratix3			21	16								2	
StratixGX		23	23	16								2	
Stratix2GX			22	16								2	
Max2		23	23	16								2	
Max3000a	18	18		16									
Max7000b	18	18		16									
Max7000ae	18	18		16									
Max7000s	18	18		16									
Spartan2		24	23	16									
Spartan2E		24	23	16									
Spartan3		24	23	16									
Spartan3A		40	39	16									
Spartan3ADSP		40	39	16									
Spartan3AN		40	39	16									
Spartan3E		40	39	16									
Spartan3L		40	39	16									
Virtex		24	23	16									
Virtex2		24	23	16									
Virtex2p		24	23	16									
VirtexE		24	23	16									
Virtex4		40	39	16									
Virtex5		14	16	16									
CoolRunner2	18			16									
CoolRunnerXpla3	18			16									
Xc9500	18			16									
Xc9500XL	18			16									
Xc9500XV	18			16									
ProAsicPlus		80											
ProAsic3		69											
ProAsic3E		72											
Fusion		69											
EC		52	51	16									
ECP		52	51	16									
ECP2		30	27	16									
ECP2M		30	27	16									
SC		56	39	16									
MACHXO		26	24										
XP		56	39	16									
XP2		28	26	16									

**FPGA Counter Resource Usage**

**CB16REB**

**16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			23	16									
Cyclone		24	23	16									1
Cyclone2		23	23	16									
Cyclone3		24	24	16									
Stratix		24	23	16									1
Stratix2		23	23	16									
Stratix3			22	16									1
StratixGX		24	24	16									1
Stratix2GX			22	16									1
Max2		24	23	16									1
Max3000a	18	18		16									
Max7000b	18	18		16									
Max7000ae	18	18		16									
Max7000s	18	18		16									
Spartan2		22	6	16									
Spartan2E		22	6	16									
Spartan3		22	6	16									
Spartan3A		42	24	16									
Spartan3ADSP		42	24	16									
Spartan3AN		42	24	16									
Spartan3E		40	22	16									
Spartan3L		40	22	16									
Virtex		22	6	16									
Virtex2		22	6	16									
Virtex2p		22	6	16									
VirtexE		22	6	16									
Virtex4		38	22	16									
Virtex5		14	17	17									
CoolRunner2	18			16									
CoolRunnerXpla3	18			16									
Xc9500	18			16									
Xc9500XL	18			16									
Xc9500XV	18			16									
ProAsicPlus		80											
ProAsic3		60											
ProAsic3E		62											
Fusion		60											
EC		58	39	16									
ECP		58	39	16									
ECP2		30	27	16									
ECP2M		30	27	16									
SC		26	24	16									
MACHXO		26	24										
XP		28	25	16									
XP2		28	26	16									

## CB16RES

### 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			23	16									
Cyclone		24	23	16									1
Cyclone2		23	23	16									
Cyclone3		24	24	16									
Stratix		24	23	16									1
Stratix2		23	23	16									
Stratix3			22	16									1
StratixGX		24	24	16									1
Stratix2GX			22	16									1
Max2		24	23	16									1
Max3000a	18	18		16									
Max7000b	18	18		16									
Max7000ae	18	18		16									
Max7000s	18	18		16									
Spartan2		22	6	16									
Spartan2E		22	6	16									
Spartan3		22	6	16									
Spartan3A		42	24	16									
Spartan3ADSP		42	24	16									
Spartan3AN		42	24	16									
Spartan3E		40	22	16									
Spartan3L		40	22	16									
Virtex		22	6	16									
Virtex2		22	6	16									
Virtex2p		22	6	16									
VirtexE		22	6	16									
Virtex4		38	22	16									
Virtex5		16	17	17									
CoolRunner2	18			16									
CoolRunnerXpla3	18			16									
Xc9500	18			16									
Xc9500XL	18			16									
Xc9500XV	18			16									
ProAsicPlus		80											
ProAsic3		60											
ProAsic3E		62											
Fusion		60											
EC		58	39	16									
ECP		58	39	16									
ECP2		30	27	16									
ECP2M		30	27	16									
SC		26	24	16									
MACHXO		26	24										
XP		28	25	16									
XP2		28	26	16									

**FPGA Counter Resource Usage**

**CB16RLEB**

**16-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			22	16									
Cyclone		40	40	16								1	
Cyclone2		23	23	16									
Cyclone3		23	23	16									
Stratix		40	40	16								1	
Stratix2		23	23	16									
Stratix3			21	16								1	
StratixGX		40	40	16								1	
Stratix2GX			39	16								1	
Max2		23	23	16								1	
Max3000a	19	19		16									
Max7000b	19	19		16									
Max7000ae	19	19		16									
Max7000s	19	19		16									
Spartan2		24	23	16									
Spartan2E		24	23	16									
Spartan3		24	23	16									
Spartan3A		40	39	16									
Spartan3ADSP		40	39	16									
Spartan3AN		40	39	16									
Spartan3E		40	39	16									
Spartan3L		40	39	16									
Virtex		24	23	16									
Virtex2		24	23	16									
Virtex2p		24	23	16									
VirtexE		24	23	16									
Virtex4		40	39	16									
Virtex5		14	16	16									
CoolRunner2	18			16									
CoolRunnerXpla3	18			16									
Xc9500	18			16									
Xc9500XL	18			16									
Xc9500XV	18			16									
ProAsicPlus		104											
ProAsic3		85											
ProAsic3E		88											
Fusion		85											
EC		58	39	16									
ECP		58	39	16									
ECP2		64	44	16									
ECP2M		64	44	16									
SC		58	41	16									
MACHXO		58	40										
XP		62	42	16									
XP2		62	43	16									



## CB16RLES

### 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			22	16									
Cyclone		40	40	16								1	
Cyclone2		23	23	16									
Cyclone3		23	23	16									
Stratix		40	40	16								1	
Stratix2		23	23	16									
Stratix3			21	16								1	
StratixGX		40	40	16								1	
Stratix2GX			39	16								1	
Max2		23	23	16								1	
Max3000a	19	19		16									
Max7000b	19	19		16									
Max7000ae	19	19		16									
Max7000s	19	19		16									
Spartan2		24	23	16									
Spartan2E		24	23	16									
Spartan3		24	23	16									
Spartan3A		40	39	16									
Spartan3ADSP		40	39	16									
Spartan3AN		40	39	16									
Spartan3E		40	39	16									
Spartan3L		40	39	16									
Virtex		24	23	16									
Virtex2		24	23	16									
Virtex2p		24	23	16									
VirtexE		24	23	16									
Virtex4		40	39	16									
Virtex5		14	16	16									
CoolRunner2	18			16									
CoolRunnerXpla3	18			16									
Xc9500	18			16									
Xc9500XL	18			16									
Xc9500XV	18			16									
ProAsicPlus		104											
ProAsic3		85											
ProAsic3E		88											
Fusion		85											
EC		58	39	16									
ECP		58	39	16									
ECP2		64	44	16									
ECP2M		64	44	16									
SC		58	41	16									
MACHXO		58	40										
XP		62	42	16									
XP2		62	43	16									

**FPGA Counter Resource Usage**

**CB32CEB**

**32-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear,  
Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			42	32									
Cyclone		44	44	32								2	
Cyclone2		44	44	32									
Cyclone3		44	44	32									
Stratix		44	44	32								2	
Stratix2		42	42	32									
Stratix3			42	32								2	
StratixGX		44	44	32								2	
Stratix2GX			40	32								2	
Max2		44	44	32								2	
Max3000a	34	34		32									
Max7000b	34	34		32									
Max7000ae	34	34		32									
Max7000s	34	34		32									
Spartan2		44	12	32									
Spartan2E		44	12	32									
Spartan3		44	12	32									
Spartan3A		94	57	34									
Spartan3ADSP		94	57	34									
Spartan3AN		94	57	34									
Spartan3E		76	41	32									
Spartan3L		76	41	32									
Virtex		44	12	32									
Virtex2		44	12	32									
Virtex2p		44	12	32									
VirtexE		44	12	32									
Virtex4		76	44	32									
Virtex5		34	33	33									
CoolRunner2	39			32									
CoolRunnerXpla3	102			32									
Xc9500	34			32									
Xc9500XL	34			32									
Xc9500XV	34			32									
ProAsicPlus		134											
ProAsic3		113											
ProAsic3E		113											
Fusion		110											
EC		46	44	32									
ECP		46	44	32									
ECP2		50	47	32									
ECP2M		50	47	32									
SC		44	44	32									
MACHXO		44	44										
XP		44	44	32									
XP2		48	46	32									

## CB32CLEB

### 32-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			43	32									
Cyclone		45	45	32									2
Cyclone2		45	45	32									
Cyclone3		45	45	32									
Stratix		45	45	32									2
Stratix2		43	43	32									
Stratix3			44	32									2
StratixGX		45	45	32									2
Stratix2GX			42	32									2
Max2		45	45	32									2
Max3000a	34	34		32									
Max7000b	34	34		32									
Max7000ae	34	34		32									
Max7000s	34	34		32									
Spartan2		46	45	32									
Spartan2E		46	45	32									
Spartan3		46	45	32									
Spartan3A		74	74	32									
Spartan3ADSP		74	74	32									
Spartan3AN		74	74	32									
Spartan3E		74	74	32									
Spartan3L		74	74	32									
Virtex		46	45	32									
Virtex2		46	45	32									
Virtex2p		46	45	32									
VirtexE		46	45	32									
Virtex4		78	77	32									
Virtex5		52	39	39									
CoolRunner2	44			32									
CoolRunnerXpla3	227			32									
Xc9500	35			32									
Xc9500XL	34			32									
Xc9500XV	34			32									
ProAsicPlus		166											
ProAsic3		148											
ProAsic3E		148											
Fusion		141											
EC	114		113	32									
ECP	114		113	32									
ECP2	52		48	32									
ECP2M	52		48	32									
SC	110		77	32									
MACHXO		48	46										
XP		110	77	32									
XP2		50	47	32									

**FPGA Counter Resource Usage**

**CB32CLEDB**

**32-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			52	32									
Cyclone		57	57	32									2
Cyclone2		57	57	32									
Cyclone3		119	119	32									
Stratix		57	57	32									2
Stratix2		51	51	32									
Stratix3			52	32									2
StratixGX		57	57	32									2
Stratix2GX			49	32									2
Max2		57	57	32									2
Max3000a	70	70		32									
Max7000b	70	70		32									
Max7000ae	70	70		32									
Max7000s	70	70		32									
Spartan2		58	56	32									
Spartan2E		58	56	32									
Spartan3		60	57	32									
Spartan3A		93	88	35									
Spartan3ADSP		93	88	35									
Spartan3AN		93	88	35									
Spartan3E		86	85	32									
Spartan3L		86	85	32									
Virtex		58	56	32									
Virtex2		60	57	32									
Virtex2p		60	57	32									
VirtexE		58	56	32									
Virtex4		90	89	32									
Virtex5		28	32	32									
CoolRunner2	40			32									
CoolRunnerXpla3	404			32									
Xc9500	37			32									
Xc9500XL	34			32									
Xc9500XV	34			32									
ProAsicPlus		302											
ProAsic3		371											
ProAsic3E		465											
Fusion		220											
EC		150	143	32									
ECP		150	143	32									
ECP2		126	92	32									
ECP2M		126	92	32									
SC		122	88	32									
MACHXO		122	90										
XP		152	103	32									
XP2		124	91	32									

**CB32REB**

**32-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			44	32									
Cyclone		46	45	32									1
Cyclone2		45	45	32									
Cyclone3		46	46	32									
Stratix		46	45	32									1
Stratix2		43	43	32									
Stratix3			45	32									1
StratixGX		46	46	32									1
Stratix2GX			42	32									1
Max2		46	45	32									1
Max3000a	34	34		32									
Max7000b	34	34		32									
Max7000ae	34	34		32									
Max7000s	34	34		32									
Spartan2		44	12	32									
Spartan2E		44	12	32									
Spartan3		44	12	32									
Spartan3A		94	57	34									
Spartan3ADSP		10	9						1				
Spartan3AN		94	57	34									
Spartan3E		76	41	32									
Spartan3L		76	41	32									
Virtex		44	12	32									
Virtex2		44	12	32									
Virtex2p		44	12	32									
VirtexE		44	12	32									
Virtex4		76	44	32									
Virtex5		6							1				
CoolRunner2	37			32									
CoolRunnerXpla3	164			32									
Xc9500	34			32									
Xc9500XL	34			32									
Xc9500XV	34			32									
ProAsicPlus		166											
ProAsic3		129											
ProAsic3E		129											
Fusion		124											
EC		112	77	32									
ECP		112	77	32									
ECP2		52	48	32									
ECP2M		52	48	32									
SC		48	46	32									
MACHXO		48	46										
XP		50	47	32									
XP2		50	47	32									

**FPGA Counter Resource Usage**

**CB32RLEB**

**32-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			43	32									
Cyclone		45	45	32									1
Cyclone2		45	45	32									
Cyclone3		45	45	32									
Stratix		45	45	32									1
Stratix2		43	43	32									
Stratix3			44	32									1
StratixGX		45	45	32									1
Stratix2GX			75	32									1
Max2		45	45	32									1
Max3000a	41	41		32									
Max7000b	41	41		32									
Max7000ae	41	41		32									
Max7000s	41	41		32									
Spartan2		46	45	32									
Spartan2E		46	45	32									
Spartan3		46	45	32									
Spartan3A		74	74	32									
Spartan3ADSP													
Spartan3AN		74	74	32									
Spartan3E		74	74	32									
Spartan3L		74	74	32									
Virtex		46	45	32									
Virtex2		46	45	32									
Virtex2p		46	45	32									
VirtexE		46	45	32									
Virtex4		78	77	32									
Virtex5		8							1				
CoolRunner2	55			32									
CoolRunnerXpla3	54			32									
Xc9500	35			32									
Xc9500XL	34			32									
Xc9500XV	34			32									
ProAsicPlus		222											
ProAsic3		180											
ProAsic3E		180											
Fusion		173											
EC		112	77	32									
ECP		112	77	32									
ECP2		118	81	32									
ECP2M		118	81	32									
SC		112	79	32									
MACHXO		112	78										
XP		116	80	32									
XP2		116	80	32									

## CD4CEB

### Cascadable BCD Counter with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	4									
Cyclone		8	7	4									2
Cyclone2		7	7	4									
Cyclone3		7	7	4									
Stratix		8	7	4									2
Stratix2		6	6	4									
Stratix3			7	4									2
StratixGX		8	8	4									2
Stratix2GX			7	4									2
Max2		6	6	4									2
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		6	6	4									
Spartan2E		6	6	4									
Spartan3		6	6	4									
Spartan3A		10	10	4									
Spartan3ADSP		10	10	4									
Spartan3AN		10	10	4									
Spartan3E		12	12	4									
Spartan3L		12	12	4									
Virtex		6	6	4									
Virtex2		6	6	4									
Virtex2p		6	6	4									
VirtexE		6	6	4									
Virtex4		10	10	4									
Virtex5		6	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		21											
ProAsic3		21											
ProAsic3E		20											
Fusion		20											
EC		10	9	4									
ECP		10	9	4									
ECP2		10	8	4									
ECP2M		10	8	4									
SC		10	8	4									
MACHXO		10	8										
XP		10	8	4									
XP2		10	8	4									

**FPGA Counter Resource Usage**

**CD4CES**

**Cascadable BCD Counter with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	4									
Cyclone		8	7	4								2	
Cyclone2		7	7	4									
Cyclone3		7	7	4									
Stratix		8	7	4								2	
Stratix2		6	6	4									
Stratix3			7	4								2	
StratixGX		8	8	4								2	
Stratix2GX			7	4								2	
Max2		6	6	4								2	
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		6	6	4									
Spartan2E		6	6	4									
Spartan3		6	6	4									
Spartan3A		10	10	4									
Spartan3ADSP		10	10	4									
Spartan3AN		10	10	4									
Spartan3E		12	12	4									
Spartan3L		12	12	4									
Virtex		6	6	4									
Virtex2		6	6	4									
Virtex2p		6	6	4									
VirtexE		6	6	4									
Virtex4		10	10	4									
Virtex5		6	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		21											
ProAsic3		21											
ProAsic3E		20											
Fusion		20											
EC		10	9	4									
ECP		10	9	4									
ECP2		10	8	4									
ECP2M		10	8	4									
SC		10	8	4									
MACHXO		10	8										
XP		10	8	4									
XP2		10	8	4									



## CD4CLEB

### Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7	4									
Cyclone	13	13	4								2	
Cyclone2	9	9	4									
Cyclone3	9	9	4									
Stratix	13	13	4								2	
Stratix2	10	10	4									
Stratix3		7	4								2	
StratixGX	13	13	4								2	
Stratix2GX		12	4								2	
Max2	13	13	4								2	
Max3000a	6	6	4									
Max7000b	6	6	4									
Max7000ae	6	6	4									
Max7000s	6	6	4									
Spartan2	14	14	4									
Spartan2E	14	14	4									
Spartan3	14	14	4									
Spartan3A	22	22	4									
Spartan3ADSP	25	24	5									
Spartan3AN	22	22	4									
Spartan3E	18	18	4									
Spartan3L	18	18	4									
Virtex	14	14	4									
Virtex2	14	14	4									
Virtex2p	14	14	4									
VirtexE	14	14	4									
Virtex4	18	18	4									
Virtex5	10	5	5									
CoolRunner2	6		4									
CoolRunnerXpla3	6		4									
Xc9500	6		4									
Xc9500XL	6		4									
Xc9500XV	6		4									
ProAsicPlus		25										
ProAsic3		26										
ProAsic3E		25										
Fusion		25										
EC		18	15	4								
ECP		18	15	4								
ECP2		12	11	4								
ECP2M		12	11	4								
SC		12	11	4								
MACHXO		12	11									
XP		12	11	4								
XP2		12	11	4								

FPGA Counter Resource Usage

CD4CLES

Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear,  
Single Pin Version

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7	4									
Cyclone	13	13	4								2	
Cyclone2	9	9	4									
Cyclone3	9	9	4									
Stratix	13	13	4								2	
Stratix2	10	10	4									
Stratix3		7	4								2	
StratixGX	13	13	4								2	
Stratix2GX		12	4								2	
Max2	13	13	4								2	
Max3000a	6	6	4									
Max7000b	6	6	4									
Max7000ae	6	6	4									
Max7000s	6	6	4									
Spartan2	16	14	4									
Spartan2E	16	14	4									
Spartan3	14	14	4									
Spartan3A	24	22	4									
Spartan3ADSP	25	24	5									
Spartan3AN	24	22	4									
Spartan3E	18	18	4									
Spartan3L	18	18	4									
Virtex	16	14	4									
Virtex2	14	14	4									
Virtex2p	14	14	4									
VirtexE	16	14	4									
Virtex4	18	18	4									
Virtex5	8	5	5									
CoolRunner2	6		4									
CoolRunnerXpla3	6		4									
Xc9500	6		4									
Xc9500XL	6		4									
Xc9500XV	6		4									
ProAsicPlus		25										
ProAsic3		26										
ProAsic3E		25										
Fusion		25										
EC	18	15	4									
ECP	18	15	4									
ECP2	12	11	4									
ECP2M	12	11	4									
SC	12	11	4									
MACHXO	12	11										
XP	12	11	4									
XP2	12	11	4									

**CD4REB**

**Cascadable BCD Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	4									
Cyclone		10	9	4									1
Cyclone2		10	10	4									
Cyclone3		10	10	4									
Stratix		10	9	4									1
Stratix2		9	9	4									
Stratix3			7	4									1
StratixGX		10	10	4									1
Stratix2GX			7	4									1
Max2		10	10	4									1
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		10	10	4									
Spartan2E		10	10	4									
Spartan3		10	10	4									
Spartan3A		14	13	4									
Spartan3ADSP		14	13	4									
Spartan3AN		14	13	4									
Spartan3E		16	15	4									
Spartan3L		14	14	4									
Virtex		10	10	4									
Virtex2		10	10	4									
Virtex2p		10	10	4									
VirtexE		10	10	4									
Virtex4		14	14	4									
Virtex5		6	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		21											
ProAsic3		22											
ProAsic3E		21											
Fusion		21											
EC		16	12	4									
ECP		16	12	4									
ECP2		12	10	4									
ECP2M		12	10	4									
SC		12	10	4									
MACHXO		12	10										
XP		12	10	4									
XP2		12	10	4									

**FPGA Counter Resource Usage**

**CD4RES**

**Cascadable BCD Counter with Clock Enable and Synchronous Reset, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	4									
Cyclone		10	9	4									1
Cyclone2		10	10	4									
Cyclone3		10	10	4									
Stratix		10	9	4									1
Stratix2		9	9	4									
Stratix3			7	4									1
StratixGX		10	10	4									1
Stratix2GX			7	4									1
Max2		10	10	4									1
Max3000a	6	6		4									
Max7000b	6	6		4									
Max7000ae	6	6		4									
Max7000s	6	6		4									
Spartan2		10	10	4									
Spartan2E		10	10	4									
Spartan3		10	10	4									
Spartan3A		14	13	4									
Spartan3ADSP		14	13	4									
Spartan3AN		14	13	4									
Spartan3E		16	15	4									
Spartan3L		14	14	4									
Virtex		10	10	4									
Virtex2		10	10	4									
Virtex2p		10	10	4									
VirtexE		10	10	4									
Virtex4		14	14	4									
Virtex5		6	4	4									
CoolRunner2	6			4									
CoolRunnerXpla3	6			4									
Xc9500	6			4									
Xc9500XL	6			4									
Xc9500XV	6			4									
ProAsicPlus		21											
ProAsic3		22											
ProAsic3E		21											
Fusion		21											
EC		16	12	4									
ECP		16	12	4									
ECP2		12	10	4									
ECP2M		12	10	4									
SC		12	10	4									
MACHXO		12	10										
XP		12	10	4									
XP2		12	10	4									

## CD4RLEB

### Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		13	4									
Cyclone		14	14	4							1	
Cyclone2		14	14	4								
Cyclone3		13	13	4								
Stratix		14	14	4							1	
Stratix2		12	12	4								
Stratix3			13	4							1	
StratixGX		14	14	4							1	
Stratix2GX			13	4							1	
Max2		14	14	4							1	
Max3000a	6	6	4									
Max7000b	6	6	4									
Max7000ae	6	6	4									
Max7000s	6	6	4									
Spartan2		16	14	4								
Spartan2E		16	14	4								
Spartan3		14	14	4								
Spartan3A		20	18	4								
Spartan3ADSP		18	18	4								
Spartan3AN		20	18	4								
Spartan3E		18	18	4								
Spartan3L		18	18	4								
Virtex		16	14	4								
Virtex2		14	14	4								
Virtex2p		14	14	4								
VirtexE		16	14	4								
Virtex4		18	18	4								
Virtex5		8	4	4								
CoolRunner2	6		4									
CoolRunnerXpla3	6		4									
Xc9500	6		4									
Xc9500XL	6		4									
Xc9500XV	6		4									
ProAsicPlus		32										
ProAsic3		27										
ProAsic3E		26										
Fusion		26										
EC		16	14	4								
ECP		16	14	4								
ECP2		14	14	4								
ECP2M		14	14	4								
SC		16	14	4								
MACHXO		14	14									
XP		14	14	4								
XP2		14	14	4								

**FPGA Counter Resource Usage**

**CD4RLES**

**Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset,  
Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		13	4									
Cyclone		14	14	4							1	
Cyclone2		14	14	4								
Cyclone3		13	13	4								
Stratix		14	14	4							1	
Stratix2		12	12	4								
Stratix3			13	4							1	
StratixGX		14	14	4							1	
Stratix2GX			13	4							1	
Max2		14	14	4							1	
Max3000a	6	6		4								
Max7000b	6	6		4								
Max7000ae	6	6		4								
Max7000s	6	6		4								
Spartan2		16	14	4								
Spartan2E		16	14	4								
Spartan3		14	14	4								
Spartan3A		20	18	4								
Spartan3ADSP		18	18	4								
Spartan3AN		20	18	4								
Spartan3E		18	18	4								
Spartan3L		18	18	4								
Virtex		16	14	4								
Virtex2		14	14	4								
Virtex2p		14	14	4								
VirtexE		16	14	4								
Virtex4		18	18	4								
Virtex5		6	4	4								
CoolRunner2	6			4								
CoolRunnerXpla3	6			4								
Xc9500	6			4								
Xc9500XL	6			4								
Xc9500XV	6			4								
ProAsicPlus		32										
ProAsic3		27										
ProAsic3E		26										
Fusion		26										
EC		16	14	4								
ECP		16	14	4								
ECP2		14	14	4								
ECP2M		14	14	4								
SC		16	14	4								
MACHXO		14	14									
XP		14	14	4								
XP2		14	14	4								

**CJ2CEB**

**2-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	2									
Cyclone		2	1	2									2
Cyclone2		1		2									
Cyclone3		2	1	2									
Stratix		2	1	2									2
Stratix2		1		2									
Stratix3				1	2								2
StratixGX		2	1	2									
Stratix2GX				1	2								2
Max2		2		2									2
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		4		2									
Spartan3A		4	2	2									
Spartan3ADSP		4	2	2									
Spartan3AN		4	2	2									
Spartan3E		4	2	2									
Spartan3L		4	2	2									
Virtex		4		2									
Virtex2		4		2									
Virtex2p		4		2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		4											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		4	1	2									
ECP		4	1	2									
ECP2		4	1	2									
ECP2M		4	1	2									
SC		4	1	2									
MACHXO		4	1										
XP		4	1	2									
XP2		4	1	2									

**FPGA Counter Resource Usage**

**CJ2CES**

**2-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		1	2									
Cyclone	2	1	2								2	
Cyclone2	1		2									
Cyclone3	2	1	2									
Stratix	2	1	2								2	
Stratix2	1		2									
Stratix3		1	2								2	
StratixGX	2	1	2								2	
Stratix2GX		1	2								2	
Max2	2		2								2	
Max3000a	2	2	2									
Max7000b	2	2	2									
Max7000ae	2	2	2									
Max7000s	2	2	2									
Spartan2	4		2									
Spartan2E	4		2									
Spartan3	4		2									
Spartan3A	4	2	2									
Spartan3ADSP	4	2	2									
Spartan3AN	4	2	2									
Spartan3E	4	2	2									
Spartan3L	4	2	2									
Virtex	4		2									
Virtex2	4		2									
Virtex2p	4		2									
VirtexE	4		2									
Virtex4	6	2	2									
Virtex5	2	2	2									
CoolRunner2	2		2									
CoolRunnerXpla3	2		2									
Xc9500	2		2									
Xc9500XL	2		2									
Xc9500XV	2		2									
ProAsicPlus	4											
ProAsic3	5											
ProAsic3E	5											
Fusion	5											
EC	4	1	2									
ECP	4	1	2									
ECP2	4	1	2									
ECP2M	4	1	2									
SC	4	1	2									
MACHXO	4	1										
XP	4	1	2									
XP2	4	1	2									



**CJ2REB**

**2-Bit Johnson Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2									1
Cyclone2		2	2	2									
Cyclone3		3	3	2									
Stratix		2	2	2									1
Stratix2		2	2	2									
Stratix3			2	2									1
StratixGX		2	2	2									1
Stratix2GX			2	2									1
Max2		2	2	2									1
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		4		2									
Spartan3A		4	2	2									
Spartan3ADSP		4	2	2									
Spartan3AN		4	2	2									
Spartan3E		4	2	2									
Spartan3L		4	2	2									
Virtex		4		2									
Virtex2		4		2									
Virtex2p		4		2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5													
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	2	2									
ECP		4	2	2									
ECP2		4	1	2									
ECP2M		4	1	2									
SC		4	1	2									
MACHXO		4	2										
XP		4	2	2									
XP2		4	1	2									

**FPGA Counter Resource Usage**

**CJ2RES**

**2-Bit Johnson Counter with Clock Enable and Synchronous Reset, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2									1
Cyclone2		2	2	2									
Cyclone3		3	3	2									
Stratix		2	2	2									1
Stratix2		2	2	2									
Stratix3			2	2									1
StratixGX		2	2	2									1
Stratix2GX			2	2									1
Max2		2	2	2									1
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4		2									
Spartan2E		4		2									
Spartan3		4		2									
Spartan3A		4	2	2									
Spartan3ADSP		4	2	2									
Spartan3AN		4	2	2									
Spartan3E		4	2	2									
Spartan3L		4	2	2									
Virtex		4		2									
Virtex2		4		2									
Virtex2p		4		2									
VirtexE		4		2									
Virtex4		6	2	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	2	2									
ECP		4	2	2									
ECP2		4	1	2									
ECP2M		4	1	2									
SC		4	1	2									
MACHXO		4	2										
XP		4	2	2									
XP2													

**CJ4CEB**

**4-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	4									
Cyclone		4	3	4									2
Cyclone2		1		4									
Cyclone3		4	1	4									
Stratix		4	3	4									2
Stratix2		1		4									
Stratix3			1	4									2
StratixGX		4	3	4									2
Stratix2GX			1	4									2
Max2		4		4									2
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		8		4									
Spartan3A		8	4	4									
Spartan3ADSP		8	4	4									
Spartan3AN		8	4	4									
Spartan3E		8	4	4									
Spartan3L		8	4	4									
Virtex		8		4									
Virtex2		8		4									
Virtex2p		8		4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		2	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		6	1	4									
ECP		6	1	4									
ECP2		6	1	4									
ECP2M		6	1	4									
SC		6	1	4									
MACHXO		6	1										
XP		6	1	4									
XP2		6	1	4									

FPGA Counter Resource Usage

CJ4CES

4-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	4								
Cyclone		4	3	4							2	
Cyclone2		1		4								
Cyclone3		4	1	4								
Stratix		4	3	4							2	
Stratix2		1		4								
Stratix3			1	4							2	
StratixGX		4	3	4							2	
Stratix2GX			1	4							2	
Max2		4		4							2	
Max3000a	4	4		4								
Max7000b	4	4		4								
Max7000ae	4	4		4								
Max7000s	4	4		4								
Spartan2		8		4								
Spartan2E		8		4								
Spartan3		8		4								
Spartan3A		8	4	4								
Spartan3ADSP		8	4	4								
Spartan3AN		8	4	4								
Spartan3E		8	4	4								
Spartan3L		8	4	4								
Virtex		8		4								
Virtex2		8		4								
Virtex2p		8		4								
VirtexE		8		4								
Virtex4		12	4	4								
Virtex5		2	4	4								
CoolRunner2	4			4								
CoolRunnerXpla3	4			4								
Xc9500	4			4								
Xc9500XL	4			4								
Xc9500XV	4			4								
ProAsicPlus		8										
ProAsic3		9										
ProAsic3E		9										
Fusion		9										
EC		6	1	4								
ECP		6	1	4								
ECP2		6	1	4								
ECP2M		6	1	4								
SC		6	1	4								
MACHXO		6	1									
XP		6	1	4								
XP2		6	1	4								

**CJ4REB**

**4-Bit Johnson Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4									1
Cyclone2		4	4	4									
Cyclone3		5	5	4									
Stratix		4	4	4									1
Stratix2		4	4	4									
Stratix3			5	4									1
StratixGX		4	4	4									1
Stratix2GX			4	4									1
Max2		4	4	4									1
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		8		4									
Spartan3A		8	4	4									
Spartan3ADSP		8	4	4									
Spartan3AN		8	4	4									
Spartan3E		8	4	4									
Spartan3L		8	4	4									
Virtex		8		4									
Virtex2		8		4									
Virtex2p		8		4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		2	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		8	4	4									
ECP		8	4	4									
ECP2		6	1	4									
ECP2M		6	1	4									
SC		6	1	4									
MACHXO		8	4										
XP		8	4	4									
XP2		6	1	4									

**FPGA Counter Resource Usage**

**CJ4RES**

**4-Bit Johnson Counter with Clock Enable and Synchronous Reset, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4									1
Cyclone2		4	4	4									
Cyclone3		5	5	4									
Stratix		4	4	4									1
Stratix2		4	4	4									
Stratix3			5	4									1
StratixGX		4	4	4									1
Stratix2GX			4	4									1
Max2		4	4	4									1
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8		4									
Spartan2E		8		4									
Spartan3		8		4									
Spartan3A		8	4	4									
Spartan3ADSP		8	4	4									
Spartan3AN		8	4	4									
Spartan3E		8	4	4									
Spartan3L		8	4	4									
Virtex		8		4									
Virtex2		8		4									
Virtex2p		8		4									
VirtexE		8		4									
Virtex4		12	4	4									
Virtex5		2	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		12											
EC		8	4	4									
ECP		8	4	4									
ECP2		6	1	4									
ECP2M		6	1	4									
SC		6	1	4									
MACHXO		8	4										
XP		8	4	4									
XP2		6	1	4									

## CJ5CEB

### 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	5									
Cyclone		5	4	5									2
Cyclone2		1		5									
Cyclone3		5	1	5									
Stratix		5	4	5									2
Stratix2		1		5									
Stratix3			1	5									2
StratixGX		5	4	5									2
Stratix2GX			1	5									2
Max2		5		5									2
Max3000a	5	5		5									
Max7000b	5	5		5									
Max7000ae	5	5		5									
Max7000s	5	5		5									
Spartan2		10		5									
Spartan2E		10		5									
Spartan3		10		5									
Spartan3A		11	5	5									
Spartan3ADSP		11	5	5									
Spartan3AN		11	5	5									
Spartan3E		11	5	5									
Spartan3L		11	5	5									
Virtex		10		5									
Virtex2		10		5									
Virtex2p		10		5									
VirtexE		10		5									
Virtex4		15	5	5									
Virtex5		4	5	5									
CoolRunner2	5			5									
CoolRunnerXpla3	5			5									
Xc9500	5			5									
Xc9500XL	5			5									
Xc9500XV	5			5									
ProAsicPlus		10											
ProAsic3		11											
ProAsic3E		11											
Fusion		11											
EC		6	1	5									
ECP		6	1	5									
ECP2		6	1	5									
ECP2M		6	1	5									
SC		6	1	5									
MACHXO		6	1										
XP		6	1	5									
XP2		6	1	5									

**FPGA Counter Resource Usage**

**CJ5CES**

**5-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	5								
Cyclone		5	4	5								2
Cyclone2		1		5								
Cyclone3		5	1	5								
Stratix		5	4	5								2
Stratix2		1		5								
Stratix3			1	5								2
StratixGX		5	4	5								2
Stratix2GX			1	5								2
Max2		5		5								2
Max3000a	5	5		5								
Max7000b	5	5		5								
Max7000ae	5	5		5								
Max7000s	5	5		5								
Spartan2		10		5								
Spartan2E		10		5								
Spartan3		10		5								
Spartan3A		11	5	5								
Spartan3ADSP		11	5	5								
Spartan3AN		11	5	5								
Spartan3E		11	5	5								
Spartan3L		11	5	5								
Virtex		10		5								
Virtex2		10		5								
Virtex2p		10		5								
VirtexE		10		5								
Virtex4		15	5	5								
Virtex5		4	5	5								
CoolRunner2	5			5								
CoolRunnerXpla3	5			5								
Xc9500	5			5								
Xc9500XL	5			5								
Xc9500XV	5			5								
ProAsicPlus		10										
ProAsic3		11										
ProAsic3E		11										
Fusion		11										
EC		6	1	5								
ECP		6	1	5								
ECP2		6	1	5								
ECP2M		6	1	5								
SC		6	1	5								
MACHXO		6	1									
XP		6	1	5								
XP2		6	1	5								



**CJ5REB**

**5-Bit Johnson Counters with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	5									
Cyclone		5	5	5									1
Cyclone2		5	5	5									
Cyclone3		6	6	5									
Stratix		5	5	5									1
Stratix2		5	5	5									
Stratix3			6	5									1
StratixGX		5	5	5									1
Stratix2GX			5	5									1
Max2		5	5	5									1
Max3000a	5	5		5									
Max7000b	5	5		5									
Max7000ae	5	5		5									
Max7000s	5	5		5									
Spartan2		10		5									
Spartan2E		10		5									
Spartan3		10		5									
Spartan3A		11	5	5									
Spartan3ADSP		11	5	5									
Spartan3AN		11	5	5									
Spartan3E		11	5	5									
Spartan3L		11	5	5									
Virtex		10		5									
Virtex2		10		5									
Virtex2p		10		5									
VirtexE		10		5									
Virtex4		15	5	5									
Virtex5		4	5	5									
CoolRunner2	5			5									
CoolRunnerXpla3	5			5									
Xc9500	5			5									
Xc9500XL	5			5									
Xc9500XV	5			5									
ProAsicPlus		15											
ProAsic3		15											
ProAsic3E		15											
Fusion		15											
EC		10	5	5									
ECP		10	5	5									
ECP2		6	1	5									
ECP2M		6	1	5									
SC		6	1	5									
MACHXO		10	5										
XP		10	5	5									
XP2													

**FPGA Counter Resource Usage**

**CJ5RES**

**5-Bit Johnson Counters with Clock Enable and Synchronous Reset, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	5									
Cyclone		5	5	5									1
Cyclone2		5	5	5									
Cyclone3		6	6	5									
Stratix		5	5	5									1
Stratix2		5	5	5									
Stratix3			6	5									1
StratixGX		5	5	5									1
Stratix2GX			5	5									1
Max2		5	5	5									1
Max3000a	5	5		5									
Max7000b	5	5		5									
Max7000ae	5	5		5									
Max7000s	5	5		5									
Spartan2		10		5									
Spartan2E		10		5									
Spartan3		10		5									
Spartan3A		11	5	5									
Spartan3ADSP		11	5	5									
Spartan3AN		11	5	5									
Spartan3E		11	5	5									
Spartan3L		11	5	5									
Virtex		10		5									
Virtex2		10		5									
Virtex2p		10		5									
VirtexE		10		5									
Virtex4		15	5	5									
Virtex5		4	5	5									
CoolRunner2	5			5									
CoolRunnerXpla3	5			5									
Xc9500	5			5									
Xc9500XL	5			5									
Xc9500XV	5			5									
ProAsicPlus		15											
ProAsic3		15											
ProAsic3E		15											
Fusion		15											
EC		10	5	5									
ECP		10	5	5									
ECP2		6	1	5									
ECP2M		6	1	5									
SC		6	1	5									
MACHXO		10	5										
XP		10	5	5									
XP2		6	1	5									

**CJ8CEB**

**8-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	8									
Cyclone		8	7	8									2
Cyclone2		1		8									
Cyclone3		8	1	8									
Stratix		8	7	8									2
Stratix2		1		8									
Stratix3			1	8									2
StratixGX		8	7	8									2
Stratix2GX			1	8									2
Max2		8		8									2
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		16		8									
Spartan3A		16	8	8									
Spartan3ADSP		16	8	8									
Spartan3AN		16	8	8									
Spartan3E		16	8	8									
Spartan3L		16	8	8									
Virtex		16		8									
Virtex2		16		8									
Virtex2p		16		8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		4	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		16											
ProAsic3		17											
ProAsic3E		17											
Fusion		17											
EC		10	1	8									
ECP		10	1	8									
ECP2		10	1	8									
ECP2M		10	1	8									
SC		10	1	8									
MACHXO		10	1										
XP		10	1	8									
XP2		10	1	8									

**FPGA Counter Resource Usage**

**CJ8CES**

**8-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		1	8									
Cyclone		8	7	8							2	
Cyclone2		1	8									
Cyclone3		8	1	8								
Stratix		8	7	8							2	
Stratix2		1	8									
Stratix3		1	8								2	
StratixGX		8	7	8							2	
Stratix2GX		1	8								2	
Max2		8	8								2	
Max3000a	8	8	8									
Max7000b	8	8	8									
Max7000ae	8	8	8									
Max7000s	8	8	8									
Spartan2		16	8									
Spartan2E		16	8									
Spartan3		16	8									
Spartan3A		16	8	8								
Spartan3ADSP		16	8	8								
Spartan3AN		16	8	8								
Spartan3E		16	8	8								
Spartan3L		16	8	8								
Virtex		16	8									
Virtex2		16	8									
Virtex2p		16	8									
VirtexE		16	8									
Virtex4		24	8	8								
Virtex5		4	8	8								
CoolRunner2	8		8									
CoolRunnerXpla3	8		8									
Xc9500	8		8									
Xc9500XL	8		8									
Xc9500XV	8		8									
ProAsicPlus		16										
ProAsic3		17										
ProAsic3E		17										
Fusion		17										
EC		10	1	8								
ECP		10	1	8								
ECP2		10	1	8								
ECP2M		10	1	8								
SC		10	1	8								
MACHXO		10	1									
XP		10	1	8								
XP2		10	1	8								

**CJ8REB**

**8-Bit Johnson Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	8									
Cyclone		9	1	8									1
Cyclone2		2	1	8									
Cyclone3		8	2	8									
Stratix		9	1	8									1
Stratix2		8	8	8									
Stratix3			2	8									1
StratixGX		9	1	8									1
Stratix2GX			2	8									1
Max2		9	1	8									1
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		16		8									
Spartan3A		16	8	8									
Spartan3ADSP		16	8	8									
Spartan3AN		16	8	8									
Spartan3E		16	8	8									
Spartan3L		16	8	8									
Virtex		16		8									
Virtex2		16		8									
Virtex2p		16		8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		4	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		10	1	8									
ECP2M		10	1	8									
SC		10	1	8									
MACHXO		16	8										
XP		16	8	8									
XP2		10	1	8									

FPGA Counter Resource Usage

**CJ8RES**

**8-Bit Johnson Counter with Clock Enable and Synchronous Reset, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	8									
Cyclone		9	1	8									1
Cyclone2		2	1	8									
Cyclone3		8	2	8									
Stratix		9	1	8									1
Stratix2		8	8	8									
Stratix3			2	8									1
StratixGX		9	1	8									1
Stratix2GX			2	8									1
Max2		9	1	8									1
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		16		8									
Spartan2E		16		8									
Spartan3		16		8									
Spartan3A		16	8	8									
Spartan3ADSP		16	8	8									
Spartan3AN		16	8	8									
Spartan3E		16	8	8									
Spartan3L		16	8	8									
Virtex		16		8									
Virtex2		16		8									
Virtex2p		16		8									
VirtexE		16		8									
Virtex4		24	8	8									
Virtex5		4	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		24											
ProAsic3		24											
ProAsic3E		24											
Fusion		24											
EC		16	8	8									
ECP		16	8	8									
ECP2		10	1	8									
ECP2M		10	1	8									
SC		10	1	8									
MACHXO		16	8										
XP		16	8	8									
XP2		10	1	8									

## CJ16CEB

### 16-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		16	15	16									2
Cyclone2		1		16									
Cyclone3		16	1	16									
Stratix		16	15	16									2
Stratix2		1		16									
Stratix3			1	16									2
StratixGX		16	15	16									
Stratix2GX			1	16									2
Max2		16		16									2
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		32		16									
Spartan3A		32	16	16									
Spartan3ADSP		32	16	16									
Spartan3AN		32	16	16									
Spartan3E		32	16	16									
Spartan3L		32	16	16									
Virtex		32		16									
Virtex2		32		16									
Virtex2p		32		16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		8	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		33											
ProAsic3E		36											
Fusion		33											
EC		18	1	16									
ECP		18	1	16									
ECP2		18	1	16									
ECP2M		18	1	16									
SC		18	1	16									
MACHXO		18	1										
XP		18	1	16									
XP2		18	1	16									

**FPGA Counter Resource Usage**

**CJ16CES**

**16-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	16									
Cyclone		16	15	16								2	
Cyclone2		1		16									
Cyclone3		16	1	16									
Stratix		16	15	16								2	
Stratix2		1		16									
Stratix3			1	16								2	
StratixGX		16	15	16									
Stratix2GX			1	16								2	
Max2		16		16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		32		16									
Spartan3A		32	16	16									
Spartan3ADSP		32	16	16									
Spartan3AN		32	16	16									
Spartan3E		32	16	16									
Spartan3L		32	16	16									
Virtex		32		16									
Virtex2		32		16									
Virtex2p		32		16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		8	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		32											
ProAsic3		33											
ProAsic3E		36											
Fusion		33											
EC		18	1	16									
ECP		18	1	16									
ECP2		18	1	16									
ECP2M		18	1	16									
SC		18	1	16									
MACHXO		18	1										
XP		18	1	16									
XP2													



**CJ16REB**

**16-Bit Johnson Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	16									
Cyclone		17	1	16									1
Cyclone2		2	1	16									
Cyclone3		16	2	16									
Stratix		17	1	16									1
Stratix2		2	1	16									
Stratix3			2	16									1
StratixGX		17	1	16									
Stratix2GX			2	16									1
Max2		17	1	16									1
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		32		16									
Spartan3A		32	16	16									
Spartan3ADSP		32	16	16									
Spartan3AN		32	16	16									
Spartan3E		32	16	16									
Spartan3L		32	16	16									
Virtex		32		16									
Virtex2		32		16									
Virtex2p		32		16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		8	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		48											
ProAsic3		48											
ProAsic3E		51											
Fusion		48											
EC		32	16	16									
ECP		32	16	16									
ECP2		18	1	16									
ECP2M		18	1	16									
SC		18	1	16									
MACHXO		32	16										
XP		32	16	16									
XP2		18	1	16									

**FPGA Counter Resource Usage**

**CJ16RES**

**16-Bit Johnson Counter with Clock Enable and Synchronous Reset, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	16									
Cyclone		17	1	16									1
Cyclone2		2	1	16									
Cyclone3		16	2	16									
Stratix		17	1	16									1
Stratix2		2	1	16									
Stratix3			2	16									1
StratixGX		17	1	16									1
Stratix2GX			2	16									1
Max2		17	1	16									1
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		32		16									
Spartan2E		32		16									
Spartan3		32		16									
Spartan3A		32	16	16									
Spartan3ADSP		32	16	16									
Spartan3AN		32	16	16									
Spartan3E		32	16	16									
Spartan3L		32	16	16									
Virtex		32		16									
Virtex2		32		16									
Virtex2p		32		16									
VirtexE		32		16									
Virtex4		48	16	16									
Virtex5		8	16	16									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		48											
ProAsic3		48											
ProAsic3E		51											
Fusion		48											
EC		32	16	16									
ECP		32	16	16									
ECP2		18	1	16									
ECP2M		18	1	16									
SC		18	1	16									
MACHXO		32	16										
XP		32	16	16									
XP2		18	1	16									

## CJ32CEB

### 32-Bit Johnson Counter with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	32									
Cyclone		32		32									2
Cyclone2		1		32									
Cyclone3		32	1	32									
Stratix		32		32									2
Stratix2		1		32									
Stratix3			1	32									2
StratixGX		32		32									2
Stratix2GX			1	32									2
Max2		32		32									2
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		64		32									
Spartan2E		64		32									
Spartan3		64		32									
Spartan3A		64	32	32									
Spartan3ADSP		64	32	32									
Spartan3AN		64	32	32									
Spartan3E		64	32	32									
Spartan3L		64	32	32									
Virtex		64		32									
Virtex2		64		32									
Virtex2p		64		32									
VirtexE		64		32									
Virtex4		96	32	32									
Virtex5		16	32	32									
CoolRunner2	32			32									
CoolRunnerXpla3	32			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		64											
ProAsic3		71											
ProAsic3E		71											
Fusion		65											
EC	34		1	32									
ECP	34		1	32									
ECP2	34		1	32									
ECP2M	34		1	32									
SC	34		1	32									
MACHXO	34		1										
XP	34		1	32									
XP2	34		1	32									

**FPGA Counter Resource Usage**

**CJ32REB**

**32-Bit Johnson Counter with Clock Enable and Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	32									
Cyclone		33	1	32									1
Cyclone2		2	1	32									
Cyclone3		32	2	32									
Stratix		33	1	32									1
Stratix2		2	1	32									
Stratix3			3	32									1
StratixGX		33	1	32									1
Stratix2GX			3	32									1
Max2		33	1	32									1
Max3000a		32	32	32									
Max7000b		32	32	32									
Max7000ae		32	32	32									
Max7000s		32	32	32									
Spartan2			64	32									
Spartan2E			64	32									
Spartan3			64	32									
Spartan3A			64	32	32								
Spartan3ADSP			64	32	32								
Spartan3AN			64	32	32								
Spartan3E			64	32	32								
Spartan3L			64	32	32								
Virtex			64	32									
Virtex2			64	32									
Virtex2p			64	32									
VirtexE			64	32									
Virtex4			96	32	32								
Virtex5			16	32	32								
CoolRunner2		32		32									
CoolRunnerXpla3		32		32									
Xc9500		32		32									
Xc9500XL		32		32									
Xc9500XV		32		32									
ProAsicPlus			96										
ProAsic3			102										
ProAsic3E			102										
Fusion			96										
EC			64	32	32								
ECP			64	32	32								
ECP2			34	1	32								
ECP2M			34	1	32								
SC			34	1	32								
MACHXO			64	32									
XP			64	32	32								
XP2			34	1	32								

CR2CEB

2-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								2	
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2								2	
Stratix2		2	2	2									
Stratix3			2	2								2	
StratixGX		2	2	2								2	
Stratix2GX			2	2								2	
Max2		2	2	2								2	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		4	4	2									
Spartan3ADSP		4	4	2									
Spartan3AN		4	4	2									
Spartan3E		4	4	2									
Spartan3L		4	4	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		4	4	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		5											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	2	2									
ECP		4	2	2									
ECP2		4	2	2									
ECP2M		4	2	2									
SC		4	2	2									
MACHXO		4	2										
XP		4	2	2									
XP2		4	2	2									

**FPGA Counter Resource Usage**

**CR2CES**

**2-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2								2	
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2								2	
Stratix2		2	2	2									
Stratix3			2	2								2	
StratixGX		2	2	2								2	
Stratix2GX			2	2								2	
Max2		2	2	2								2	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		2	2	2									
Spartan2E		2	2	2									
Spartan3		2	2	2									
Spartan3A		4	4	2									
Spartan3ADSP		4	4	2									
Spartan3AN		4	4	2									
Spartan3E		4	4	2									
Spartan3L		4	4	2									
Virtex		2	2	2									
Virtex2		2	2	2									
Virtex2p		2	2	2									
VirtexE		2	2	2									
Virtex4		4	4	2									
Virtex5		2	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		5											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4	2	2									
ECP		4	2	2									
ECP2		4	2	2									
ECP2M		4	2	2									
SC		4	2	2									
MACHXO		4	2										
XP		4	2	2									
XP2		4	2	2									

CR4CEB

4-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								2	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								2	
Stratix2		4	4	4									
Stratix3			4	4								2	
StratixGX		4	4	4								2	
Stratix2GX			4	4								2	
Max2		5	5	4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		6	5	4									
Spartan2E		6	5	4									
Spartan3		6	5	4									
Spartan3A		10	8	4									
Spartan3ADSP		10	9	4									
Spartan3AN		10	8	4									
Spartan3E		10	9	4									
Spartan3L		10	9	4									
Virtex		6	5	4									
Virtex2		6	5	4									
Virtex2p		6	5	4									
VirtexE		6	5	4									
Virtex4		10	9	4									
Virtex5		2	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		11											
ProAsic3		10											
ProAsic3E		10											
Fusion		10											
EC		4	4	4									
ECP		4	4	4									
ECP2		8	4	4									
ECP2M		8	4	4									
SC		8	4	4									
MACHXO		8	4										
XP		8	4	4									
XP2		8	4	4									

**FPGA Counter Resource Usage**

**CR4CES**

**4-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								2	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								2	
Stratix2		4	4	4									
Stratix3			4	4								2	
StratixGX		4	4	4								2	
Stratix2GX			4	4								2	
Max2		5	5	4								2	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		6	5	4									
Spartan2E		6	5	4									
Spartan3		6	5	4									
Spartan3A		10	8	4									
Spartan3ADSP		10	9	4									
Spartan3AN		10	8	4									
Spartan3E		10	9	4									
Spartan3L		10	9	4									
Virtex		6	5	4									
Virtex2		6	5	4									
Virtex2p		6	5	4									
VirtexE		6	5	4									
Virtex4		10	9	4									
Virtex5		2	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		11											
ProAsic3		10											
ProAsic3E		10											
Fusion		10											
EC		4	4	4									
ECP		4	4	4									
ECP2		8	4	4									
ECP2M		8	4	4									
SC		8	4	4									
MACHXO		8	4										
XP		8	4	4									
XP2		8	4	4									



**CR8CEB**

**8-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								2	
Cyclone2		8	8	8									
Cyclone3		8	8	8									
Stratix		8	8	8								2	
Stratix2		9	9	8									
Stratix3			8	8								2	
StratixGX		8	8	8								2	
Stratix2GX			8	8								2	
Max2		8	8	8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8		8									
Spartan2E		8		8									
Spartan3		8		8									
Spartan3A	18	8		8									
Spartan3ADSP	18	15		8									
Spartan3AN	18	15		8									
Spartan3E	18	8		8									
Spartan3L	18	8		8									
Virtex		8		8									
Virtex2		8		8									
Virtex2p		8		8									
VirtexE		8		8									
Virtex4		16	8	8									
Virtex5		6	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		25											
ProAsic3		20											
ProAsic3E		20											
Fusion		20											
EC	8	8		8									
ECP	8	8		8									
ECP2	14	12		8									
ECP2M	14	12		8									
SC	8	8		8									
MACHXO	8	8											
XP	8	8		8									
XP2	12	11		8									

**FPGA Counter Resource Usage**

**CR8CES**

**8-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			8	8									
Cyclone		8	8	8								2	
Cyclone2		8	8	8									
Cyclone3		8	8	8									
Stratix		8	8	8								2	
Stratix2		9	9	8									
Stratix3			8	8								2	
StratixGX		8	8	8								2	
Stratix2GX			8	8								2	
Max2		8	8	8								2	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		8		8									
Spartan2E		8		8									
Spartan3		8		8									
Spartan3A	18	8		8									
Spartan3ADSP	18	15		8									
Spartan3AN	18	15		8									
Spartan3E	18	8		8									
Spartan3L	18	8		8									
Virtex		8		8									
Virtex2		8		8									
Virtex2p		8		8									
VirtexE		8		8									
Virtex4		16	8	8									
Virtex5		6	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		25											
ProAsic3		20											
ProAsic3E		20											
Fusion		20											
EC	8	8		8									
ECP	8	8		8									
ECP2	14	12		8									
ECP2M	14	12		8									
SC	8	8		8									
MACHXO	8	8											
XP	8	8		8									
XP2	12	11		8									

**CR16CEB**

**16-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16	16										
Cyclone		16	16	16								2	
Cyclone2		16	16	16									
Cyclone3		16	16	16									
Stratix		16	16	16								2	
Stratix2		17	17	16									
Stratix3			16	16								2	
StratixGX		16	16	16								2	
Stratix2GX			16	16								2	
Max2		16	16	16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16		16									
Spartan2E		16		16									
Spartan3		16		16									
Spartan3A		36	18	16									
Spartan3ADSP		36	18	16									
Spartan3AN		36	18	16									
Spartan3E		34	16	16									
Spartan3L		34	16	16									
Virtex		16		16									
Virtex2		16		16									
Virtex2p		16		16									
VirtexE		16		16									
Virtex4		32	16	16									
Virtex5		14	17	17									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		55											
ProAsic3		44											
ProAsic3E		46											
Fusion		44											
EC		16	16	16									
ECP		16	16	16									
ECP2		22	20	16									
ECP2M		22	20	16									
SC		16	16	16									
MACHXO		16	16										
XP		16	16	16									
XP2		20	19	16									

**FPGA Counter Resource Usage**

**CR16CES**

**16-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16	16										
Cyclone		16	16	16								2	
Cyclone2		16	16	16									
Cyclone3		16	16	16									
Stratix		16	16	16								2	
Stratix2		17	17	16									
Stratix3			16	16								2	
StratixGX		16	16	16								2	
Stratix2GX			16	16								2	
Max2		16	16	16								2	
Max3000a	16	16		16									
Max7000b	16	16		16									
Max7000ae	16	16		16									
Max7000s	16	16		16									
Spartan2		16		16									
Spartan2E		16		16									
Spartan3		16		16									
Spartan3A		36	18	16									
Spartan3ADSP		36	18	16									
Spartan3AN		36	18	16									
Spartan3E		34	16	16									
Spartan3L		34	16	16									
Virtex		16		16									
Virtex2		16		16									
Virtex2p		16		16									
VirtexE		16		16									
Virtex4		32	16	16									
Virtex5		14	17	17									
CoolRunner2	16			16									
CoolRunnerXpla3	16			16									
Xc9500	16			16									
Xc9500XL	16			16									
Xc9500XV	16			16									
ProAsicPlus		55											
ProAsic3		44											
ProAsic3E		46											
Fusion		44											
EC		16	16	16									
ECP		16	16	16									
ECP2		22	20	16									
ECP2M		22	20	16									
SC		16	16	16									
MACHXO		16	16										
XP		16	16	16									
XP2		20	19	16									

## CR32CEB

### 32-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			32	32									
Cyclone		32	32	32								2	
Cyclone2		32	32	32									
Cyclone3		32	32	32									
Stratix		32	32	32								2	
Stratix2		33	33	32									
Stratix3			32	32								2	
StratixGX		32	32	32								2	
Stratix2GX			32	32								2	
Max2		32	32	32								2	
Max3000a	32	32		32									
Max7000b	32	32		32									
Max7000ae	32	32		32									
Max7000s	32	32		32									
Spartan2		32		32									
Spartan2E		32		32									
Spartan3		32		32									
Spartan3A	84	48		34									
Spartan3ADSP	84	48		34									
Spartan3AN	84	48		34									
Spartan3E	66	32		32									
Spartan3L	66	32		32									
Virtex	32			32									
Virtex2	32			32									
Virtex2p	32			32									
VirtexE	32			32									
Virtex4	64	32		32									
Virtex5	26	33		33									
CoolRunner2	36			32									
CoolRunnerXpla3	98			32									
Xc9500	32			32									
Xc9500XL	32			32									
Xc9500XV	32			32									
ProAsicPlus		117											
ProAsic3	96												
ProAsic3E	96												
Fusion	93												
EC	32	32		32									
ECP	32	32		32									
ECP2	38	36		32									
ECP2M	38	36		32									
SC	32	32		32									
MACHXO	32	32											
XP	32	32		32									
XP2	36	35		32									

## Tools Utilized

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The following vendor device tools were used to determine the resource usage statistics:

### **Actel**

Actel Designer Software Version 6.2

### **Altera**

Quartus II 5.0

### **Lattice**

ispLEVER 5.0

### **Xilinx**

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

## Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1

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