FPGA Clock Manager Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Clock Manager cores.

Core Reference
CR0128 (v1.10) July 17, 2008

Clock Manager

The available Clock Manager cores are listed as follows:

CLKMAN_1 *CLKMAN_2* *CLKMAN_3* *CLKMAN_4*

CLKMAN_1

Single Operational Output Clock Manager

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone										1		2	
Cyclone2										1		2	
Cyclone3										1			
Stratix										1		2	
Stratix2										1		2	
StratixGX										1		2	
Max2													
Max3000a													
Max7000b													
Max7000ae													
Max7000s													
Spartan2											1	3	
Spartan2E											1	3	
Spartan3												3	1
Spartan3A													
Spartan3E												3	1
Spartan3L													
Virtex											1	3	
Virtex2												3	1
Virtex2p												3	1
VirtexE											1	3	
Virtex4												3	1
Virtex5													
CoolRunner2													
CoolRunnerXpla3													
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus													
ProAsic3													
ProAsic3E													
EC										1			
ECP										1			
ECP2													
ECP2M													
MACHXO													
XP										1			

CLKMAN_2

Dual Operational Output Clock Manager

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone										1		3	
Cyclone2										1		3	
Cyclone3										1			
Stratix										1		3	
Stratix2										1		3	
StratixGX										1		3	
Max2													
Max3000a													
Max7000b													
Max7000ae													
Max7000s													
Spartan2											1	4	
Spartan2E											1	4	
Spartan3												4	1
Spartan3A													
Spartan3E												4	1
Spartan3L													
Virtex											1	4	
Virtex2												4	1
Virtex2p												4	1
VirtexE											1	4	
Virtex4												4	1
Virtex5													
CoolRunner2													
CoolRunnerXpla3													
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus													
ProAsic3													
ProAsic3E													
EC										1			
ECP										1			
ECP2													
ECP2M													
MACHXO													
XP										1			

CLKMAN_3

Multiple Operational Output Clock Manager

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone										1		3	
Cyclone2										1		3	
Cyclone3										1			
Stratix										1		3	
Stratix2										1		3	
StratixGX										1		4	
Max2													
Max3000a													
Max7000b													
Max7000ae													
Max7000s													
Spartan2											1	5	
Spartan2E											1	5	
Spartan3												5	1
Spartan3A													
Spartan3E												5	1
Spartan3L													
Virtex											1	5	
Virtex2												5	1
Virtex2p												5	1
VirtexE											1	5	
Virtex4												5	1
Virtex5													
CoolRunner2													
CoolRunnerXpla3													
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus													
ProAsic3													
ProAsic3E													
EC										1			
ECP										1			
ECP2													
ECP2M													
MACHXO													
XP										1			

CLKMAN_4

Multiple Operational Output Clock Manager

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Cyclone										1		3	
Cyclone2										1		3	
Cyclone3										1			
Stratix										1		3	
Stratix2										1		3	
StratixGX										1		4	
Max2													
Max3000a													
Max7000b													
Max7000ae													
Max7000s													
Spartan2											1	6	
Spartan2E											1	6	
Spartan3												6	1
Spartan3A													
Spartan3E												6	1
Spartan3L													
Virtex											1	6	
Virtex2												6	1
Virtex2p												6	1
VirtexE											1	6	
Virtex4												6	1
Virtex5													
CoolRunner2													
CoolRunnerXpla3													
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus													
ProAsic3													
ProAsic3E													
EC										1			
ECP										1			
ECP2													
ECP2M													
MACHXO													
XP										1			

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1