FPGA Clock Divider Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Clock Divider cores.

Core Reference
CR0127 (v1.11) December 19, 2008

Clock Divider

The available Clock Divider cores are listed as follows:

CDIV2
CDIV2DC50
CDIV3
CDIV4
CDIV4DC50
CDIV5
CDIV6
CDIV6DC50
CDIV7
CDIV8
CDIV8DC50
CDIV9
CDIV10
CDIV10DC50
CDIV12
CDIV12DC50
CDIV16
CDIV16DC50
CDIV20
CDIV20DC50
CDIV24
CDIV24DC50
CDIV32
CDIV32DC50
CDIV64
CDIV64DC50
CDIV128
CDIV128DC50
CDIV256
CDIV256DC50
CDIVN_8
CDIVN_16
CDIVN_32

CDIV2

Clock Divider by 2

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1		1									
Cyclone2		1		1									
Cyclone3		1	1	1									
Stratix		1		1									
Stratix2		1		1									
Stratix3			1	1									
StratixGX		1		1									
Stratix2GX			1	1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1									
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		2	1	1									
CoolRunner2	3			3									
CoolRunnerXpla3	3			3									
Xc9500	3			3									
Xc9500XL	3			3									
Xc9500XV	3			3									
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

CDIV2DC50

Clock Divider by 2 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	1									
Cyclone		1		1									
Cyclone2		1		1									
Cyclone3		1	1	1									
Stratix		1		1									
Stratix2		1		1									
Stratix3			1	1									
StratixGX		1		1									
Stratix2GX			1	1									
Max2		1		1									
Max3000a	1	1		1									
Max7000b	1	1		1									
Max7000ae	1	1		1									
Max7000s	1	1		1									
Spartan2		2		1									
Spartan2E		2		1									
Spartan3		2		1									
Spartan3A		3	1	1									
Spartan3ADSP		3	1	1									
Spartan3AN		3	1	1									
Spartan3E		3	1	1									
Spartan3L		3	1	1									
Virtex		2		1									
Virtex2		2		1									
Virtex2p		2		1									
VirtexE		2		1									
Virtex4		3	1	1									
Virtex5		2	1	1									
CoolRunner2	1			1									
CoolRunnerXpla3	1			1									
Xc9500	1			1									
Xc9500XL	1			1									
Xc9500XV	1			1									
ProAsicPlus		1											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2	1	1									
ECP		2	1	1									
ECP2		2	1	1									
ECP2M		2	1	1									
SC		2	1	1									
MACHXO		2	1										
XP		2	1	1									
XP2		2	1	1									

CDIV3

Clock Divider by 3

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			1	2									
Cyclone		2	1	2								1	
Cyclone2		1	1	2									
Cyclone3		2	1	2									
Stratix		2	1	2								1	
Stratix2		1	1	2									
Stratix3			1	2								1	
StratixGX		2	1	2								1	
Stratix2GX			1	2								1	
Max2		2	1	2								1	
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4	1	2									
Spartan2E		4	1	2									
Spartan3		4	1	2									
Spartan3A		6	3	2									
Spartan3ADSP		6	3	2									
Spartan3AN		6	3	2									
Spartan3E		6	3	2									
Spartan3L		6	3	2									
Virtex		4	1	2									
Virtex2		4	1	2									
Virtex2p		4	1	2									
VirtexE		4	1	2									
Virtex4		6	3	2									
Virtex5		4	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		3											
ProAsic3		3											
ProAsic3E		3											
Fusion		3											
EC		4	1	2									
ECP		4	1	2									
ECP2		4	1	2									
ECP2M		4	1	2									
SC		4	1	2									
MACHXO		4	1										
XP		4	1	2									
XP2		4	1	2									

CDIV4

Clock Divider by 4

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	3									
Cyclone		3	2	3								1	
Cyclone2		3	2	3									
Cyclone3		3	3	3									
Stratix		3	2	3								1	
Stratix2		3	2	3									
Stratix3			3	4								1	
StratixGX		3	2	3								1	
Stratix2GX			3	3								1	
Max2		3	2	3								1	
Max3000a	3	3		3									
Max7000b	3	3		3									
Max7000ae	3	3		3									
Max7000s	3	3		3									
Spartan2		3	2	2									
Spartan2E		3	2	2									
Spartan3		3	2	2									
Spartan3A		4	3	2									
Spartan3ADSP		4	4	2									
Spartan3AN		4	3	2									
Spartan3E		4	3	2									
Spartan3L		4	3	2									
Virtex		3	2	2									
Virtex2		3	2	2									
Virtex2p		3	2	2									
VirtexE		3	2	2									
Virtex4		7	4	3									
Virtex5		5	1	2									
CoolRunner2	3			3									
CoolRunnerXpla3	3			3									
Xc9500	3			3									
Xc9500XL	3			3									
Xc9500XV	3			3									
ProAsicPlus		5											
ProAsic3		6											
ProAsic3E		6											
Fusion		5											
EC		4	3	3									
ECP		4	3	3									
ECP2		4	3	3									
ECP2M		4	3	3									
SC		4	3	3									
MACHXO		4	3										
XP		4	3	3									
XP2		4	3	3									

CDIV4DC50

Clock Divider by 4 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	3									
Cyclone		3	2	3								1	
Cyclone2		3	2	3									
Cyclone3		3	3	3									
Stratix		3	2	3								1	
Stratix2		3	2	3									
Stratix3			3	3								1	
StratixGX		3	2	3								1	
Stratix2GX			3	3								1	
Max2		3	2	3								1	
Max3000a	3	3		3									
Max7000b	3	3		3									
Max7000ae	3	3		3									
Max7000s	3	3		3									
Spartan2		6		3									
Spartan2E		6		3									
Spartan3		6	1	3									
Spartan3A		9	4	3									
Spartan3ADSP		9	4	3									
Spartan3AN		9	4	3									
Spartan3E		9	4	3									
Spartan3L		9	4	3									
Virtex		6		3									
Virtex2		6	1	3									
Virtex2p		6	1	3									
VirtexE		6		3									
Virtex4		9	4	3									
Virtex5		4	3	3									
CoolRunner2	3			3									
CoolRunnerXpla3	3			3									
Xc9500	3			3									
Xc9500XL	3			3									
Xc9500XV	3			3									
ProAsicPlus		5											
ProAsic3		6											
ProAsic3E		6											
Fusion		6											
EC		4	3	3									
ECP		4	3	3									
ECP2		6	2	3									
ECP2M		6	2	3									
SC		6	2	3									
MACHXO		4	3										
XP		4	3	3									
XP2		6	2	3									

CDIV5

Clock Divider by 5

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3			4	4								1	
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		7	5	3									
Spartan2E		7	5	3									
Spartan3		5	5	3									
Spartan3A		15	10	5									
Spartan3ADSP		12	10	4									
Spartan3AN		15	10	5									
Spartan3E		7	7	3									
Spartan3L		9	7	3									
Virtex		7	5	3									
Virtex2		5	5	3									
Virtex2p		5	5	3									
VirtexE		7	5	3									
Virtex4		10	8	4									
Virtex5		5	1	3									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		11											
ProAsic3		8											
ProAsic3E		8											
Fusion		7											
EC		6	4	4									
ECP		6	4	4									
ECP2		8	5	4									
ECP2M		8	5	4									
SC		8	5	4									
MACHXO		6	4										
XP		6	4	4									
XP2		8	5	4									

CDIV6

Clock Divider by 6

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	3	4								1	
Cyclone2		4	3	4									
Cyclone3		4	4	4									
Stratix		4	3	4								1	
Stratix2		4	3	4									
Stratix3			4	4								1	
StratixGX		4	3	4								1	
Stratix2GX			4	4								1	
Max2		4	3	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		7	5	3									
Spartan2E		7	5	3									
Spartan3		7	5	3									
Spartan3A		12	8	4									
Spartan3ADSP		12	8	4									
Spartan3AN		12	8	4									
Spartan3E		9	7	3									
Spartan3L		9	7	3									
Virtex		7	5	3									
Virtex2		7	5	3									
Virtex2p		7	5	3									
VirtexE		7	5	3									
Virtex4		12	8	4									
Virtex5		5	1	3									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		9											
ProAsic3		8											
ProAsic3E		8											
Fusion		7											
EC		6	4	4									
ECP		6	4	4									
ECP2		8	5	4									
ECP2M		8	5	4									
SC		8	5	4									
MACHXO		6	4										
XP		6	4	4									
XP2		8	5	4									

CDIV6DC50

Clock Divider by 6 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	3									
Cyclone		5	5	4								1	
Cyclone2		4	4	4									
Cyclone3		3	3	3									
Stratix		5	5	4								1	
Stratix2		3	3	3									
Stratix3			3	4								1	
StratixGX		3	3	3								1	
Stratix2GX			3	3								1	
Max2		3	3	3								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8	3	4									
Spartan2E		8	3	4									
Spartan3		8	3	4									
Spartan3A		9	6	3									
Spartan3ADSP		10	8	4									
Spartan3AN		9	6	3									
Spartan3E		12	7	4									
Spartan3L		9	5	3									
Virtex		8	3	4									
Virtex2		8	4	4									
Virtex2p		8	3	4									
VirtexE		8	3	4									
Virtex4		12	7	4									
Virtex5		4	3	3									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		11											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		6	4	4									
ECP		6	4	4									
ECP2		6	3	3									
ECP2M		6	3	3									
SC		6	3	3									
MACHXO		6	5										
XP		6	5	4									
XP2		6	3	3									

CDIV7

Clock Divider by 7

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3			4	4								1	
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		7	4	3									
Spartan2E		7	4	3									
Spartan3		7	5	3									
Spartan3A		7	7	3									
Spartan3ADSP		7	7	3									
Spartan3AN		7	7	3									
Spartan3E		9	7	3									
Spartan3L		7	7	3									
Virtex		7	4	3									
Virtex2		7	5	3									
Virtex2p		7	5	3									
VirtexE		7	4	3									
Virtex4		10	8	4									
Virtex5		5	1	3									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		10											
ProAsic3		8											
ProAsic3E		8											
Fusion		7											
EC		6	4	4									
ECP		6	4	4									
ECP2		6	4	4									
ECP2M		6	4	4									
SC		6	4	4									
MACHXO		6	4										
XP		6	4	4									
XP2		6	4	4									

CDIV8

Clock Divider by 8

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	3	4									
Stratix3			4	4								1	
StratixGX		4	4	4									
Stratix2GX			4	4								1	
Max2		4	3	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		5	4	3									
Spartan2E		5	4	3									
Spartan3		5	4	3									
Spartan3A		7	6	3									
Spartan3ADSP		7	6	3									
Spartan3AN		7	6	3									
Spartan3E		7	6	3									
Spartan3L		7	6	3									
Virtex		5	4	3									
Virtex2		5	4	3									
Virtex2p		5	4	3									
VirtexE		5	4	3									
Virtex4		10	7	4									
Virtex5		5	1	3									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		8											
ProAsic3		8											
ProAsic3E		8											
Fusion		7											
EC		6	5	5									
ECP		6	5	5									
ECP2		6	4	4									
ECP2M		6	4	4									
SC		6	4	4									
MACHXO		6	4										
XP		6	4	4									
XP2		6	4	4									

CDIV8DC50

Clock Divider by 8 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	3	4								1	
Cyclone2		4	3	4									
Cyclone3		4	4	4									
Stratix		4	3	4								1	
Stratix2		4	3	4									
Stratix3			4	4								1	
StratixGX		4	3	4								1	
Stratix2GX			4	4								1	
Max2		4	3	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		6	4	4									
Spartan2E		6	4	4									
Spartan3		6	4	4									
Spartan3A		16	10	6									
Spartan3ADSP		13	8	5									
Spartan3AN		16	10	6									
Spartan3E		10	8	4									
Spartan3L		10	8	4									
Virtex		6	4	4									
Virtex2		6	4	4									
Virtex2p		6	4	4									
VirtexE		6	4	4									
Virtex4		10	8	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		11											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		6	4	4									
ECP		6	4	4									
ECP2		6	5	4									
ECP2M		6	5	4									
SC		6	5	4									
MACHXO		6	5										
XP		6	5	4									
XP2		6	5	4									

CDIV9

Clock Divider by 9

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	5									
Cyclone		5	5	5								1	
Cyclone2		5	5	5									
Cyclone3		5	5	5									
Stratix		5	5	5								1	
Stratix2		5	5	5									
Stratix3			5	6								1	
StratixGX		5	5	5								1	
Stratix2GX			5	5								1	
Max2		5	5	5								1	
Max3000a	5	5		5									
Max7000b	5	5		5									
Max7000ae	5	5		5									
Max7000s	5	5		5									
Spartan2		7	7	4									
Spartan2E		7	7	4									
Spartan3		7	6	4									
Spartan3A		10	9	4									
Spartan3ADSP		13	12	5									
Spartan3AN		10	9	4									
Spartan3E		10	9	4									
Spartan3L		10	9	4									
Virtex		7	7	4									
Virtex2		7	6	4									
Virtex2p		7	6	4									
VirtexE		7	7	4									
Virtex4		13	10	5									
Virtex5		5	1	4									
CoolRunner2	5			5									
CoolRunnerXpla3	5			5									
Xc9500	5			5									
Xc9500XL	5			5									
Xc9500XV	5			5									
ProAsicPlus		15											
ProAsic3		14											
ProAsic3E		13											
Fusion		12											
EC		6	5	5									
ECP		6	5	5									
ECP2		8	6	5									
ECP2M		8	6	5									
SC													
MACHXO		6	5										
XP		6	5	5									
XP2		8	6	5									

CDIV10

Clock Divider by 10

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	5									
Cyclone		5	4	5								1	
Cyclone2		5	4	5									
Cyclone3		5	5	5									
Stratix		5	4	5								1	
Stratix2		5	4	5									
Stratix3			5	6								1	
StratixGX		5	4	5								1	
Stratix2GX			5	5								1	
Max2		5	4	5								1	
Max3000a	5	5		5									
Max7000b	5	5		5									
Max7000ae	5	5		5									
Max7000s	5	5		5									
Spartan2		9	6	4									
Spartan2E		9	6	4									
Spartan3		9	6	4									
Spartan3A		10	8	4									
Spartan3ADSP		15	10	5									
Spartan3AN		10	8	4									
Spartan3E		12	9	4									
Spartan3L		12	9	4									
Virtex		9	6	4									
Virtex2		9	6	4									
Virtex2p		9	6	4									
VirtexE		9	6	4									
Virtex4		13	10	5									
Virtex5		5	1	4									
CoolRunner2	5			5									
CoolRunnerXpla3	5			5									
Xc9500	5			5									
Xc9500XL	5			5									
Xc9500XV	5			5									
ProAsicPlus		14											
ProAsic3		14											
ProAsic3E		13											
Fusion		12											
EC		6	5	5									
ECP		6	5	5									
ECP2		8	6	5									
ECP2M		8	6	5									
SC		8	6	5									
MACHXO		6	5										
XP		6	5	5									
XP2		8	6	5									

CDIV10DC50

Clock Divider by 10 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4								1	
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4								1	
Stratix2		4	4	4									
Stratix3			4	4								1	
StratixGX		4	4	4								1	
Stratix2GX			4	4								1	
Max2		4	4	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		6	3	4									
Spartan2E		6	3	4									
Spartan3		6	3	4									
Spartan3A		17	14	7									
Spartan3ADSP		17	14	7									
Spartan3AN		17	14	7									
Spartan3E		10	7	4									
Spartan3L		10	7	4									
Virtex		6	3	4									
Virtex2		6	3	4									
Virtex2p		6	3	4									
VirtexE		6	3	4									
Virtex4		10	7	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		12											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		6	4	4									
ECP		6	4	4									
ECP2		6	4	4									
ECP2M		6	4	4									
SC		6	4	4									
MACHXO		6	5										
XP		6	5	4									
XP2		6	4	4									

CDIV12

Clock Divider by 12

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	5									
Cyclone		5	4	5								1	
Cyclone2		5	4	5									
Cyclone3		5	5	5									
Stratix		5	4	5								1	
Stratix2		5	4	5									
Stratix3			5	6								1	
StratixGX		5	4	5								1	
Stratix2GX			5	5								1	
Max2		5	4	5								1	
Max3000a	5	5		5									
Max7000b	5	5		5									
Max7000ae	5	5		5									
Max7000s	5	5		5									
Spartan2		7	6	4									
Spartan2E		7	6	4									
Spartan3		7	6	4									
Spartan3A		14	11	6									
Spartan3ADSP		8	8	4									
Spartan3AN		14	11	6									
Spartan3E		10	9	4									
Spartan3L		10	9	4									
Virtex		7	6	4									
Virtex2		7	6	4									
Virtex2p		7	6	4									
VirtexE		7	6	4									
Virtex4		13	10	5									
Virtex5		5	1	4									
CoolRunner2	5			5									
CoolRunnerXpla3	5			5									
Xc9500	5			5									
Xc9500XL	5			5									
Xc9500XV	5			5									
ProAsicPlus		13											
ProAsic3		13											
ProAsic3E		13											
Fusion		12											
EC		6	5	5									
ECP		6	5	5									
ECP2		8	6	5									
ECP2M		8	6	5									
SC		8	6	5									
MACHXO		6	5										
XP		6	5	5									
XP2		8	6	5									

CDIV12DC50

Clock Divider by 12 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	3	4								1	
Cyclone2		4	3	4									
Cyclone3		4	4	4									
Stratix		4	3	4								1	
Stratix2		4	3	4									
Stratix3			4	4								1	
StratixGX		4	3	4								1	
Stratix2GX			4	4								1	
Max2		4	3	4								1	
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		8	3	4									
Spartan2E		8	3	4									
Spartan3		10	4	4									
Spartan3A		17	9	5									
Spartan3ADSP		17	9	5									
Spartan3AN		17	9	5									
Spartan3E		14	8	4									
Spartan3L		14	8	4									
Virtex		8	3	4									
Virtex2		10	4	4									
Virtex2p		10	4	4									
VirtexE		8	3	4									
Virtex4		14	7	4									
Virtex5		4	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		11											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		6	4	4									
ECP		6	4	4									
ECP2		6	5	4									
ECP2M		6	5	4									
SC		6	5	4									
MACHXO		6	5										
XP		6	5	4									
XP2		6	5	4									

CDIV16

Clock Divider by 16

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	5									
Cyclone		5	5	5								1	
Cyclone2		5	5	5									
Cyclone3		5	5	5									
Stratix		5	5	5								1	
Stratix2		5	4	5									
Stratix3			5	5								1	
StratixGX		5	5	5								1	
Stratix2GX			5	5								1	
Max2		5	4	5								1	
Max3000a	5	5		5									
Max7000b	5	5		5									
Max7000ae	5	5		5									
Max7000s	5	5		5									
Spartan2		5	5	4									
Spartan2E		5	5	4									
Spartan3		5	5	4									
Spartan3A		8	8	4									
Spartan3ADSP		8	8	4									
Spartan3AN		8	8	4									
Spartan3E		8	8	4									
Spartan3L		8	8	4									
Virtex		5	5	4									
Virtex2		5	5	4									
Virtex2p		5	5	4									
VirtexE		5	5	4									
Virtex4		11	9	5									
Virtex5		5	1	4									
CoolRunner2	5			5									
CoolRunnerXpla3	5			5									
Xc9500	5			5									
Xc9500XL	5			5									
Xc9500XV	5			5									
ProAsicPlus		12											
ProAsic3		12											
ProAsic3E		12											
Fusion		11											
EC		6	5	5									
ECP		6	5	5									
ECP2		6	5	5									
ECP2M		6	5	5									
SC		6	5	5									
MACHXO		6	5										
XP		6	5	5									
XP2		6	5	5									

CDIV16DC50

Clock Divider by 16 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	5									
Cyclone		6	5	5								1	
Cyclone2		6	5	5									
Cyclone3		6	6	5									
Stratix		6	5	5								1	
Stratix2		5	4	5									
Stratix3			5	6								1	
StratixGX		6	5	5								1	
Stratix2GX			5	5								1	
Max2		6	5	5								1	
Max3000a	5	5		5									
Max7000b	5	5		5									
Max7000ae	5	5		5									
Max7000s	5	5		5									
Spartan2		8	5	5									
Spartan2E		8	5	5									
Spartan3		8	5	5									
Spartan3A		20	15	8									
Spartan3ADSP		15	12	7									
Spartan3AN		20	15	8									
Spartan3E		13	10	5									
Spartan3L		13	9	5									
Virtex		8	5	5									
Virtex2		8	5	5									
Virtex2p		8	5	5									
VirtexE		8	5	5									
Virtex4		13	10	5									
Virtex5		4	5	5									
CoolRunner2	5			5									
CoolRunnerXpla3	5			5									
Xc9500	5			5									
Xc9500XL	5			5									
Xc9500XV	5			5									
ProAsicPlus		14											
ProAsic3		13											
ProAsic3E		14											
Fusion		13											
EC		6	6	5									
ECP		6	6	5									
ECP2		8	7	5									
ECP2M		8	7	5									
SC		8	6	5									
MACHXO		8	7										
XP		8	7	5									
XP2		8	7	5									

CDIV20

Clock Divider by 20

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	6									
Cyclone		10	9	6								1	
Cyclone2		7	6	6									
Cyclone3		8	8	6									
Stratix		9	8	6								1	
Stratix2		6	5	6									
Stratix3			6	6								1	
StratixGX		9	8	6									
Stratix2GX			6	6								1	
Max2		8	7	6								1	
Max3000a	6	6		6									
Max7000b	6	6		6									
Max7000ae	6	6		6									
Max7000s	6	6		6									
Spartan2		9	9	5									
Spartan2E		9	9	5									
Spartan3		9	9	5									
Spartan3A		13	10	5									
Spartan3ADSP		15	14	5									
Spartan3AN		13	10	5									
Spartan3E		13	13	5									
Spartan3L		13	13	5									
Virtex		9	9	5									
Virtex2		9	9	5									
Virtex2p		9	9	5									
VirtexE		9	9	5									
Virtex4		16	14	6									
Virtex5		5	1	5									
CoolRunner2	6			6									
CoolRunnerXpla3	6			6									
Xc9500	6			6									
Xc9500XL	6			6									
Xc9500XV	6			6									
ProAsicPlus		18											
ProAsic3		18											
ProAsic3E		16											
Fusion		15											
EC		8	7	6									
ECP		8	7	6									
ECP2		10	9	6									
ECP2M		10	9	6									
SC		10	9	6									
MACHXO		10	10										
XP		10	9	6									
XP2		10	9	6									

CDIV20DC50

Clock Divider by 20 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	5									
Cyclone		6	5	5								1	
Cyclone2		6	5	5									
Cyclone3		6	6	5									
Stratix		6	5	5								1	
Stratix2		5	4	5									
Stratix3			5	6								1	
StratixGX		6	5	5								1	
Stratix2GX			5	5								1	
Max2		6	5	5								1	
Max3000a	5	5		5									
Max7000b	5	5		5									
Max7000ae	5	5		5									
Max7000s	5	5		5									
Spartan2		10	4	5									
Spartan2E		10	4	5									
Spartan3		10	4	5									
Spartan3A		19	16	7									
Spartan3ADSP		19	16	9									
Spartan3AN		19	14	7									
Spartan3E		15	9	5									
Spartan3L		15	9	5									
Virtex		10	4	5									
Virtex2		10	4	5									
Virtex2p		10	4	5									
VirtexE		10	4	5									
Virtex4		15	9	5									
Virtex5		4	5	5									
CoolRunner2	5			5									
CoolRunnerXpla3	5			5									
Xc9500	5			5									
Xc9500XL	5			5									
Xc9500XV	5			5									
ProAsicPlus		15											
ProAsic3		14											
ProAsic3E		15											
Fusion		14											
EC		6	6	5									
ECP		6	6	5									
ECP2		10	6	5									
ECP2M		10	6	5									
SC		10	6	5									
MACHXO		8	7										
XP		8	7	5									
XP2		10	6	5									

CDIV24

Clock Divider by 24

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	6									
Cyclone		9	8	6								1	
Cyclone2		7	6	6									
Cyclone3		8	8	6									
Stratix		8	7	6								1	
Stratix2		6	5	6									
Stratix3			6	6								1	
StratixGX		8	7	6								1	
Stratix2GX			6	6								1	
Max2		8	7	6								1	
Max3000a	6	6		6									
Max7000b	6	6		6									
Max7000ae	6	6		6									
Max7000s	6	6		6									
Spartan2		11	9	5									
Spartan2E		11	9	5									
Spartan3		11	9	5									
Spartan3A		13	10	5									
Spartan3ADSP		15	13	5									
Spartan3AN		13	10	5									
Spartan3E		15	13	5									
Spartan3L		15	13	5									
Virtex		11	9	5									
Virtex2		11	9	5									
Virtex2p		11	9	5									
VirtexE		11	9	5									
Virtex4		18	14	6									
Virtex5		7	1	5									
CoolRunner2	6			6									
CoolRunnerXpla3	6			6									
Xc9500	6			6									
Xc9500XL	6			6									
Xc9500XV	6			6									
ProAsicPlus		17											
ProAsic3		17											
ProAsic3E		15											
Fusion		14											
EC		8	7	6									
ECP		8	7	6									
ECP2		12	9	6									
ECP2M		12	9	6									
SC		12	9	6									
MACHXO		10	9										
XP		10	9	6									
XP2		12	9	6									

CDIV24DC50

Clock Divider by 24 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			5	5									
Cyclone		6	5	5								1	
Cyclone2		6	5	5									
Cyclone3		6	6	5									
Stratix		6	5	5								1	
Stratix2		5	4	5									
Stratix3			5	5								1	
StratixGX		6	5	5								1	
Stratix2GX			5	5								1	
Max2		7	6	6								1	
Max3000a	5	5		5									
Max7000b	5	5		5									
Max7000ae	5	5		5									
Max7000s	5	5		5									
Spartan2		6	4	5									
Spartan2E		6	4	5									
Spartan3		8	4	5									
Spartan3A		19	12	7									
Spartan3ADSP		19	13	7									
Spartan3AN		19	12	7									
Spartan3E		13	9	5									
Spartan3L		13	9	5									
Virtex		6	4	5									
Virtex2		8	4	5									
Virtex2p		8	4	5									
VirtexE		6	4	5									
Virtex4		13	9	5									
Virtex5		4	5	5									
CoolRunner2	5			5									
CoolRunnerXpla3	5			5									
Xc9500	5			5									
Xc9500XL	5			5									
Xc9500XV	5			5									
ProAsicPlus		15											
ProAsic3		14											
ProAsic3E		15											
Fusion		14											
EC		6	6	5									
ECP		6	6	5									
ECP2		6	6	5									
ECP2M		6	6	5									
SC		6	6	5									
MACHXO		8	7										
XP		8	7	5									
XP2		6	6	5									

CDIV32

Clock Divider by 32

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	6									
Cyclone		7	7	6								1	
Cyclone2		7	7	6									
Cyclone3		7	7	6									
Stratix		7	7	6								1	
Stratix2		6	5	6									
Stratix3			6	6								1	
StratixGX		7	7	6								1	
Stratix2GX			6	6								1	
Max2		8	7	6								1	
Max3000a	6	6		6									
Max7000b	6	6		6									
Max7000ae	6	6		6									
Max7000s	6	6		6									
Spartan2		7	7	5									
Spartan2E		7	7	5									
Spartan3		9	7	5									
Spartan3A		11	11	5									
Spartan3ADSP		13	12	5									
Spartan3AN		11	11	5									
Spartan3E		11	11	5									
Spartan3L		11	11	5									
Virtex		7	7	5									
Virtex2		9	7	5									
Virtex2p		9	7	5									
VirtexE		7	7	5									
Virtex4		14	12	6									
Virtex5		9	1	5									
CoolRunner2	6			6									
CoolRunnerXpla3	6			6									
Xc9500	6			6									
Xc9500XL	6			6									
Xc9500XV	6			6									
ProAsicPlus		16											
ProAsic3		15											
ProAsic3E		15											
Fusion		14											
EC		8	8	7									
ECP		8	8	7									
ECP2		12	9	6									
ECP2M		12	9	6									
SC		8	7	6									
MACHXO		10	9										
XP		8	8	7									
XP2		10	8	6									

CDIV32DC50

Clock Divider by 32 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	6									
Cyclone		8	7	6								1	
Cyclone2		8	7	6									
Cyclone3		8	8	6									
Stratix		8	7	6								1	
Stratix2		7	6	6									
Stratix3			6	7								1	
StratixGX		8	7	6								1	
Stratix2GX			6	6								1	
Max2		8	7	6								1	
Max3000a	6	6		6									
Max7000b	6	6		6									
Max7000ae	6	6		6									
Max7000s	6	6		6									
Spartan2		10	7	6									
Spartan2E		10	7	6									
Spartan3		10	7	6									
Spartan3A		24	18	10									
Spartan3ADSP		22	21	10									
Spartan3AN		24	18	10									
Spartan3E		16	14	6									
Spartan3L		16	13	6									
Virtex		10	7	6									
Virtex2		10	7	6									
Virtex2p		10	7	6									
VirtexE		10	7	6									
Virtex4		16	13	6									
Virtex5		6	9	9									
CoolRunner2	6			6									
CoolRunnerXpla3	6			6									
Xc9500	6			6									
Xc9500XL	6			6									
Xc9500XV	6			6									
ProAsicPlus		19											
ProAsic3		17											
ProAsic3E		17											
Fusion		17											
EC		8	8	6									
ECP		8	8	6									
ECP2		8	8	6									
ECP2M		8	8	6									
SC		8	8	6									
MACHXO		10	9										
XP		12	10	6									
XP2		8	8	6									

CDIV64

Clock Divider by 64

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	7									
Cyclone		8	8	7								1	
Cyclone2		8	8	7									
Cyclone3		8	8	7									
Stratix		8	8	7								1	
Stratix2		8	8	7									
Stratix3			7	7								1	
StratixGX		8	8	7								1	
Stratix2GX			7	7								1	
Max2		8	8	7								1	
Max3000a	7	7		7									
Max7000b	7	7		7									
Max7000ae	7	7		7									
Max7000s	7	7		7									
Spartan2		9	9	6									
Spartan2E		9	9	6									
Spartan3		11	9	6									
Spartan3A		14	14	6									
Spartan3ADSP		14	14	6									
Spartan3AN		14	14	6									
Spartan3E		14	14	6									
Spartan3L		14	14	6									
Virtex		9	9	6									
Virtex2		11	9	6									
Virtex2p		11	9	6									
VirtexE		9	9	6									
Virtex4		15	15	7									
Virtex5		7	1	6									
CoolRunner2	7			7									
CoolRunnerXpla3	7			7									
Xc9500	7			7									
Xc9500XL	7			7									
Xc9500XV	7			7									
ProAsicPlus		20											
ProAsic3		19											
ProAsic3E		19											
Fusion		18											
EC		8	8	7									
ECP		8	8	7									
ECP2		14	12	7									
ECP2M		14	12	7									
SC		8	8	7									
MACHXO		12	10										
XP		10	9	7									
XP2													

CDIV64DC50

Clock Divider by 64 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9	7									
Cyclone		10	9	7								1	
Cyclone2		10	9	7									
Cyclone3		10	10	7									
Stratix		10	9	7								1	
Stratix2		9	8	7									
Stratix3			9	7								1	
StratixGX		10	9	7								1	
Stratix2GX			9	7								1	
Max2		10	9	7								1	
Max3000a	7	7		7									
Max7000b	7	7		7									
Max7000ae	7	7		7									
Max7000s	7	7		7									
Spartan2		12	8	7									
Spartan2E		12	8	7									
Spartan3		12	9	7									
Spartan3A		19	19	7									
Spartan3ADSP		23	22	9									
Spartan3AN		19	19	7									
Spartan3E		19	15	7									
Spartan3L		19	16	7									
Virtex		12	8	7									
Virtex2		12	9	7									
Virtex2p		10	8	7									
VirtexE		12	8	7									
Virtex4		19	15	7									
Virtex5		8	11	11									
CoolRunner2	7			7									
CoolRunnerXpla3	7			7									
Xc9500	7			7									
Xc9500XL	7			7									
Xc9500XV	7			7									
ProAsicPlus		22											
ProAsic3		20											
ProAsic3E		21											
Fusion		21											
EC		12	10	7									
ECP		12	10	7									
ECP2		10	10	7									
ECP2M		10	10	7									
SC		12	11	7									
MACHXO		12	11										
XP		12	11	7									
XP2		10	10	7									

CDIV128

Clock Divider by 128

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			9	8									
Cyclone		9	9	8								1	
Cyclone2		9	9	8									
Cyclone3		9	9	8									
Stratix		9	9	8								1	
Stratix2		9	9	8									
Stratix3			9	8								1	
StratixGX		9	9	8								1	
Stratix2GX			9	8								1	
Max2		9	9	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		11	10	7									
Spartan2E		11	10	7									
Spartan3		13	10	7									
Spartan3A		17	16	7									
Spartan3ADSP		17	16	7									
Spartan3AN		17	16	7									
Spartan3E		17	16	7									
Spartan3L		17	16	7									
Virtex		11	10	7									
Virtex2		13	10	7									
Virtex2p		13	10	7									
VirtexE		11	10	7									
Virtex4		18	17	8									
Virtex5		7	1	7									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		25											
ProAsic3		24											
ProAsic3E		24											
Fusion		23											
EC		10	10	9									
ECP		10	10	9									
ECP2		14	12	8									
ECP2M		14	12	8									
SC		10	10	8									
MACHXO		12	11										
XP		10	10	9									
XP2		12	11	8									

CDIV128DC50

Clock Divider by 128 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10	8									
Cyclone		12	11	8								1	
Cyclone2		12	11	8									
Cyclone3		12	12	8									
Stratix		12	11	8								1	
Stratix2		10	9	8									
Stratix3			10	8								1	
StratixGX		12	11	8								1	
Stratix2GX			10	8								1	
Max2		12	11	8								1	
Max3000a	8	8		8									
Max7000b	8	8		8									
Max7000ae	8	8		8									
Max7000s	8	8		8									
Spartan2		12	2	8									
Spartan2E		12	2	8									
Spartan3		12	9	8									
Spartan3A		26	26	8									
Spartan3ADSP		24	23	8									
Spartan3AN		26	26	8									
Spartan3E		20	10	8									
Spartan3L		20	10	8									
Virtex		12	2	8									
Virtex2		12	9	8									
Virtex2p		12	9	8									
VirtexE		12	2	8									
Virtex4		20	17	8									
Virtex5		8	8	8									
CoolRunner2	8			8									
CoolRunnerXpla3	8			8									
Xc9500	8			8									
Xc9500XL	8			8									
Xc9500XV	8			8									
ProAsicPlus		27											
ProAsic3		25											
ProAsic3E		26											
Fusion		25											
EC		12	12	8									
ECP		12	12	8									
ECP2		18	14	8									
ECP2M		18	14	8									
SC		12	11	8									
MACHXO		20	13										
XP		14	12	8									
XP2		16	13	8									

CDIV256

Clock Divider by 256

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10	9									
Cyclone		11	11	9								1	
Cyclone2		11	11	9									
Cyclone3		11	11	9									
Stratix		11	11	9								1	
Stratix2		10	10	9									
Stratix3			10	9								1	
StratixGX		11	11	9								1	
Stratix2GX			10	9								1	
Max2		11	11	9								1	
Max3000a	9	9		9									
Max7000b	9	9		9									
Max7000ae	9	9		9									
Max7000s	9	9		9									
Spartan2		11	11	8									
Spartan2E		11	11	8									
Spartan3		13	11	8									
Spartan3A		18	18	8									
Spartan3ADSP		20	19	8									
Spartan3AN		18	18	8									
Spartan3E		18	18	8									
Spartan3L		18	18	8									
Virtex		11	11	8									
Virtex2		13	11	8									
Virtex2p		13	11	8									
VirtexE		11	11	8									
Virtex4		19	19	9									
Virtex5		7	1	8									
CoolRunner2	9			9									
CoolRunnerXpla3	9			9									
Xc9500	9			9									
Xc9500XL	9			9									
Xc9500XV	9			9									
ProAsicPlus		30											
ProAsic3		28											
ProAsic3E		28											
Fusion		27											
EC		12	11	9									
ECP		12	11	9									
ECP2		16	14	9									
ECP2M		16	14	9									
SC		10	10	9									
MACHXO		14	12										
XP		12	11	9									
XP2		14	13	9									

CDIV256DC50

Clock Divider by 256 with 50% Duty Cycle Output

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			11	9									
Cyclone		19	12	9								1	
Cyclone2		14	13	9									
Cyclone3		13	13	9									
Stratix		19	12	9								1	
Stratix2		12	11	9									
Stratix3			12	9								1	
StratixGX		19	12	9								1	
Stratix2GX			11	9								1	
Max2		13	12	9								1	
Max3000a	9	9		9									
Max7000b	9	9		9									
Max7000ae	9	9		9									
Max7000s	9	9		9									
Spartan2		14	3	9									
Spartan2E		14	3	9									
Spartan3		16	12	9									
Spartan3A		29	28	9									
Spartan3ADSP		27	27	9									
Spartan3AN		29	28	9									
Spartan3E		25	12	9									
Spartan3L		25	12	9									
Virtex		14	3	9									
Virtex2		14	12	9									
Virtex2p		14	12	9									
VirtexE		14	3	9									
Virtex4		25	21	9									
Virtex5		6	9	9									
CoolRunner2	9			9									
CoolRunnerXpla3	9			9									
Xc9500	9			9									
Xc9500XL	9			9									
Xc9500XV	9			9									
ProAsicPlus		32											
ProAsic3		30											
ProAsic3E		30											
Fusion		29											
EC		14	14	9									
ECP		14	14	9									
ECP2		20	17	9									
ECP2M		20	17	9									
SC		18	14	9									
MACHXO		22	14										
XP		16	15	9									
XP2		18	16	9									

CDIVN_8

8-Bit Programmable Clock Divider

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			15	9									
Cyclone		26	26	9								1	
Cyclone2		24	24	9									
Cyclone3		24	24	9									
Stratix		26	26	9								1	
Stratix2		24	24	9									
Stratix3			15	9								1	
StratixGX		26	26	9								1	
Stratix2GX			14	9								1	
Max2		25	25	9								1	
Max3000a	24	24		9									
Max7000b	24	24		9									
Max7000ae	24	24		9									
Max7000s	24	24		9									
Spartan2		18	16	9									
Spartan2E		18	16	9									
Spartan3		26	24	9									
Spartan3A		53	51	9									
Spartan3ADSP		45	45	9									
Spartan3AN		53	51	9									
Spartan3E		39	37	9									
Spartan3L		27	25	9									
Virtex		18	16	9									
Virtex2		26	24	9									
Virtex2p		26	24	9									
VirtexE		18	16	9									
Virtex4		35	33	9									
Virtex5		18	10	10									
CoolRunner2	10			9									
CoolRunnerXpla3	10			9									
Xc9500	10			9									
Xc9500XL	10			9									
Xc9500XV	10			9									
ProAsicPlus		53											
ProAsic3		46											
ProAsic3E		50											
Fusion		50											
EC		24	24	9									
ECP		24	24	9									
ECP2		24	20	9									
ECP2M		24	20	9									
SC		34	24	9									
MACHXO		20	19										
XP		28	28	9									
XP2		34	27	9									

CDIVN_16

16-Bit Programmable Clock Divider

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			27	17									
Cyclone		47	47	17								1	
Cyclone2		45	45	17									
Cyclone3		45	45	17									
Stratix		47	47	17								1	
Stratix2		28	28	17									
Stratix3			27	17								1	
StratixGX		47	47	17								1	
Stratix2GX			26	17								1	
Max2		46	46	17								1	
Max3000a	48	48		17									
Max7000b	48	48		17									
Max7000ae	48	48		17									
Max7000s	48	48		17									
Spartan2		32	28	17									
Spartan2E		32	28	17									
Spartan3		34	28	17									
Spartan3A		55	51	17									
Spartan3ADSP		53	50	17									
Spartan3AN		55	51	17									
Spartan3E		49	45	17									
Spartan3L		49	45	17									
Virtex		32	28	17									
Virtex2		34	28	17									
Virtex2p		34	28	17									
VirtexE		32	28	17									
Virtex4		49	45	17									
Virtex5		18	17	17									
CoolRunner2	23			17									
CoolRunnerXpla3	142			17									
Xc9500	29			17									
Xc9500XL	28			17									
Xc9500XV	28			17									
ProAsicPlus		110											
ProAsic3		96											
ProAsic3E		108											
Fusion		107											
EC		46	45	17									
ECP		46	45	17									
ECP2		36	33	17									
ECP2M		36	33	17									
SC		64	44	17									
MACHXO		32	30										
XP		74	60	17									
XP2		62	48	17									

CDIVN_32

32-Bit Programmable Clock Divider

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			52	33									
Cyclone		89	89	33								1	
Cyclone2		89	89	33									
Cyclone3		87	87	33									
Stratix		120	89	33									
Stratix2		53	53	33									
Stratix3			53	33								1	
StratixGX		89	89	33								1	
Stratix2GX			52	33								1	
Max2		88	88	33								1	
Max3000a	129	129		33									
Max7000b	129	129		33									
Max7000ae	129	129		33									
Max7000s	84	84		33									
Spartan2		62	55	33									
Spartan2E		62	55	33									
Spartan3		62	55	33									
Spartan3A		85	83	33									
Spartan3ADSP		85	83	33									
Spartan3AN		85	83	33									
Spartan3E		93	86	33									
Spartan3L		85	83	33									
Virtex		62	55	33									
Virtex2		62	55	33									
Virtex2p		62	55	33									
VirtexE		62	55	33									
Virtex4		95	88	33									
Virtex5		36	33	33									
CoolRunner2	72			33									
CoolRunnerXpla3	300			33									
Xc9500	73			33									
Xc9500XL	73			33									
Xc9500XV	73			33									
ProAsicPlus		233											
ProAsic3		386											
ProAsic3E		363											
Fusion		227											
EC		88	87	33									
ECP		88	87	33									
ECP2		64	59	33									
ECP2M		64	59	33									
SC		124	87	33									
MACHXO		60	57										
XP		148	120	33									
XP2		124	90	33									

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1