



FPGA Bus Joiner Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Bus Joiner cores.

Core Reference
CR0126 (v1.11) December 19, 2008

Bus Joiner

The available Bus Joiner cores are listed as follows:

<i>J2B2_4B</i>	<i>J3B_3S</i>	<i>J3S_3B</i>	<i>J3S_3BX</i>
<i>J4B2_8B</i>	<i>J4B4_16B</i>	<i>J4B8_32B</i>	<i>J4B_2B2</i>
<i>J4B_2B2X</i>	<i>J4B_4S</i>	<i>J4S_4B</i>	<i>J4S_4BX</i>
<i>J5B_5S</i>	<i>J5S_5B</i>	<i>J5S_5BX</i>	<i>J6B_6S</i>
<i>J6S_6B</i>	<i>J6S_6BX</i>	<i>J7B_7S</i>	<i>J7S_7B</i>
<i>J7S_7BX</i>	<i>J8B2_16B</i>	<i>J8B4_32B</i>	<i>J8B_4B2</i>
<i>J8B_4B2X</i>	<i>J8B_8S</i>	<i>J8S_8B</i>	<i>J8S_8BX</i>
<i>J9B_9S</i>	<i>J9S_9B</i>	<i>J9S_9BX</i>	<i>J10B_10S</i>
<i>J10S_10B</i>	<i>J10S_10BX</i>	<i>J12B_12S</i>	<i>J12S_12B</i>
<i>J12S_12BX</i>	<i>J16B2_32B</i>	<i>J16B_4B4</i>	<i>J16B_4B4X</i>
<i>J16B_8B2</i>	<i>J16B_8B2X</i>	<i>J16B_16S</i>	<i>J16S_16B</i>
<i>J16S_16BX</i>	<i>J32B_4B8</i>	<i>J32B_4B8X</i>	<i>J32B_8B4</i>
<i>J32B_8B4X</i>	<i>J32B_16B2</i>	<i>J32B_16B2X</i>	

FPGA Bus Joiner Resource Usage

J2B2_4B

2 x 2-Bit input bus to 1 x 4-bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

J3B_3S

3-Bit input bus to 3 Single pin outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		3											
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3		3											
StratixGX		3	3										
Stratix2gx		3											
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3											
Spartan3adsp		3											
Spartan3an		3											
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5		3	3										
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3	3										
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		3	3										
ECP2M		3	3										
Sc		3											
MACHXO		3	3										
XP		3	3										
Xp2		3											

FPGA Bus Joiner Resource Usage

J3S_3B

3 Single pin inputs to single 3-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		3											
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3		3											
StratixGX		3	3										
Stratix2gx		3											
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3											
Spartan3adsp		3											
Spartan3an		3											
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5		3	3										
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3	3										
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		3	3										
ECP2M		3	3										
Sc		3											
MACHXO		3	3										
XP		3	3										
Xp2		3											

J3S_3BX

3 Single pin IO to single 3-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		3											
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3		3											
StratixGX		3	3										
Stratix2gx		3											
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3											
Spartan3adsp		3											
Spartan3an		3											
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5		3	3										
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3	3										
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		3	3										
ECP2M		3	3										
Sc		3											
MACHXO		3	3										
XP		3	3										
Xp2		3											

FPGA Bus Joiner Resource Usage

J4B2_8B

2 x 4-Bit input bus to 1 x 8-bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

J4B4_16B

4 x 4-Bit input bus to 1 x 16-bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

FPGA Bus Joiner Resource Usage

J4B8_32B

8 x 4-Bit input bus to 1 x 32-bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

J4B_2B2

1 x 4-bit input bus to 2 x 2-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

FPGA Bus Joiner Resource Usage

J4B_2B2X

1 x 4-bit IO bus to 2 x 2-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

J4B_4S

4-Bit input bus to 4 Single pin outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

FPGA Bus Joiner Resource Usage

J4S_4B

4 Single pin inputs to single 4-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

J4S_4BX

4 Single pin IO to single 4-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a		4	4										
Max7000b		4	4										
Max7000ae		4	4										
Max7000s		4	4										
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2		4	4										
CoolRunnerXpla3		4	4										
Xc9500		4	4										
Xc9500XL		4	4										
Xc9500XV		4	4										
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

FPGA Bus Joiner Resource Usage

J5B_5S

5-Bit input bus to 5 Single pin outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		5											
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3		5											
StratixGX		5	5										
Stratix2gx		5											
Max2		5											
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A		5											
Spartan3adsp		5											
Spartan3an		5											
Spartan3E		5	5										
Spartan3L		5	5										
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5		5	5										
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5	5										
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		5	5										
ECP2M		5	5										
Sc		5											
MACHXO		5	5										
XP		5	5										
Xp2		5											

J5S_5B

5 Single pin inputs to single 5-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		5											
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3		5											
StratixGX		5	5										
Stratix2gx		5											
Max2		5											
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A		5											
Spartan3adsp		5											
Spartan3an		5											
Spartan3E		5	5										
Spartan3L		5	5										
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5		5	5										
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5	5										
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		5	5										
ECP2M		5	5										
Sc		5											
MACHXO		5	5										
XP		5	5										
Xp2		5											

FPGA Bus Joiner Resource Usage

J5S_5BX

5 Single pin IO to single 5-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		5											
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3		5											
StratixGX		5	5										
Stratix2gx		5											
Max2		5											
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A		5											
Spartan3adsp		5											
Spartan3an		5											
Spartan3E		5	5										
Spartan3L		5	5										
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5		5	5										
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5	5										
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		5	5										
ECP2M		5	5										
Sc		5											
MACHXO		5	5										
XP		5	5										
Xp2		5											

J6B_6S

6-Bit input bus to 6 Single pin outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

FPGA Bus Joiner Resource Usage

J6S_6B

6 Single pin inputs to single 6-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

J6S_6BX

6 Single pin IO to single 6-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

FPGA Bus Joiner Resource Usage

J7B_7S

7-Bit input bus to 7 Single pin outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7											
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3		7											
StratixGX		7	7										
Stratix2gx		7											
Max2		7											
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A		7											
Spartan3adsp		7											
Spartan3an		7											
Spartan3E		7	7										
Spartan3L		7	7										
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5		7	7										
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7	7										
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		7	7										
ECP2M		7	7										
Sc		7											
MACHXO		7	7										
XP		7	7										
Xp2		7											

J7S_7B

7 Single pin inputs to single 7-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7											
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3		7											
StratixGX		7	7										
Stratix2gx		7											
Max2		7											
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A		7											
Spartan3adsp		7											
Spartan3an		7											
Spartan3E		7	7										
Spartan3L		7	7										
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5		7	7										
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7	7										
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		7	7										
ECP2M		7	7										
Sc		7											
MACHXO		7	7										
XP		7	7										
Xp2		7											

FPGA Bus Joiner Resource Usage

J7S_7BX

7 Single pin IO to single 7-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7											
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3		7											
StratixGX		7	7										
Stratix2gx		7											
Max2		7											
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A		7											
Spartan3adsp		7											
Spartan3an		7											
Spartan3E		7	7										
Spartan3L		7	7										
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5		7	7										
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7	7										
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		7	7										
ECP2M		7	7										
Sc		7											
MACHXO		7	7										
XP		7	7										
Xp2		7											

J8B2_16B

2 x 8-Bit input bus to 1 x 16-bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

FPGA Bus Joiner Resource Usage

J8B4_32B

4 x 8-Bit input bus to 1 x 32-bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

J8B_4B2

1 x 8-bit input bus to 2 x 4-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

FPGA Bus Joiner Resource Usage

J8B_4B2X

1 x 8-bit IO bus to 2 x 4-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

J8B_8S

8-Bit input bus to 8 single pin outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

FPGA Bus Joiner Resource Usage

J8S_8B

8 Single pin inputs to single 8-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

J8S_8BX

8 Single pin IO to single 8-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

FPGA Bus Joiner Resource Usage

J9B_9S

9-Bit input bus to 9 Single pin outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		9											
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3		9											
StratixGX		9	9										
Stratix2gx		9											
Max2		9											
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A		9											
Spartan3adsp		9											
Spartan3an		9											
Spartan3E		9	9										
Spartan3L		9	9										
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5		9	9										
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9	9										
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		9	9										
ECP2M		9	9										
Sc		9											
MACHXO		9	9										
XP		9	9										
Xp2		9											

J9S_9B

9 Single pin inputs to single 9-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		9											
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3		9											
StratixGX		9	9										
Stratix2gx		9											
Max2		9											
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A		9											
Spartan3adsp		9											
Spartan3an		9											
Spartan3E		9	9										
Spartan3L		9	9										
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5		9	9										
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9	9										
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		9	9										
ECP2M		9	9										
Sc		9											
MACHXO		9	9										
XP		9	9										
Xp2		9											

FPGA Bus Joiner Resource Usage

J9S_9BX

9 Single pin IO to single 9-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		9											
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3		9											
StratixGX		9	9										
Stratix2gx		9											
Max2		9											
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A		9											
Spartan3adsp		9											
Spartan3an		9											
Spartan3E		9	9										
Spartan3L		9	9										
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5		9	9										
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9	9										
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		9	9										
ECP2M		9	9										
Sc		9											
MACHXO		9	9										
XP		9	9										
Xp2		9											

J10B_10S

10-Bit input bus to 10 Single pin outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a		10	10										
Max7000b		10	10										
Max7000ae		10	10										
Max7000s		10	10										
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2		10	10										
CoolRunnerXpla3		10	10										
Xc9500		10	10										
Xc9500XL		10	10										
Xc9500XV		10	10										
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

FPGA Bus Joiner Resource Usage

J10S_10B

10 Single pin inputs to single 10-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a		10	10										
Max7000b		10	10										
Max7000ae		10	10										
Max7000s		10	10										
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2		10	10										
CoolRunnerXpla3		10	10										
Xc9500		10	10										
Xc9500XL		10	10										
Xc9500XV		10	10										
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

J10S_10BX

10 Single pin IO to single 10-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a		10	10										
Max7000b		10	10										
Max7000ae		10	10										
Max7000s		10	10										
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2		10	10										
CoolRunnerXpla3		10	10										
Xc9500		10	10										
Xc9500XL		10	10										
Xc9500XV		10	10										
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

FPGA Bus Joiner Resource Usage

J12B_12S

12-Bit input bus to 12 single pin outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

J12S_12B

12 Single pin inputs to single 12-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

FPGA Bus Joiner Resource Usage

J12S_12BX

12 single-Bit IO to single 12-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a		12	12										
Max7000b		12	12										
Max7000ae		12	12										
Max7000s		12	12										
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2		12	12										
CoolRunnerXpla3		12	12										
Xc9500		12	12										
Xc9500XL		12	12										
Xc9500XV		12	12										
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

J16B2_32B

2 x 16-Bit input bus to 1 x 32-bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Bus Joiner Resource Usage

J16B_4B4

1 x 16-bit input bus to 4 x 4-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

J16B_4B4X

1 x 16-bit IO bus to 4 x 4-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Bus Joiner Resource Usage

J16B_8B2

1 x 16-bit input bus to 2 x 8-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

J16B_8B2X

1 x 16-bit IO bus to 2 x 8-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Bus Joiner Resource Usage

J16B_16S

Single 16-Bit input bus to 16 single pin outputs

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

J16S_16B

16 Single pin inputs to single 16-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

FPGA Bus Joiner Resource Usage

J16S_16BX

16 Single pin IO to single 16-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a		16	16										
Max7000b		16	16										
Max7000ae		16	16										
Max7000s		16	16										
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2		16	16										
CoolRunnerXpla3		16	16										
Xc9500		16	16										
Xc9500XL		16	16										
Xc9500XV		16	16										
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

J32B_4B8

1 x 32-Bit input bus to 8 x 4-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Bus Joiner Resource Usage

J32B_4B8X

1 x 32-Bit IO bus to 8 x 4-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		64											
Cyclone		64	64										
Cyclone2		64	64										
Cyclone3		64	64										
Stratix		64	64										
Stratix2		64	64										
Stratix3		64											
StratixGX		64	64										
Stratix2gx		64											
Max2		64											
Max3000a	64	64											
Max7000b	64	64											
Max7000ae	64	64											
Max7000s	64	64											
Spartan2		64	64										
Spartan2E		64	64										
Spartan3		64	64										
Spartan3A		64											
Spartan3adsp		64											
Spartan3an		64											
Spartan3E		64	64										
Spartan3L		64	64										
Virtex		64	64										
Virtex2		64	64										
Virtex2p		64	64										
VirtexE		64	64										
Virtex4		64	64										
Virtex5		64	64										
ProAsicPlus		64	64										
ProAsic3		64	64										
ProAsic3E		64											
Fusion		64											
EC		64	64										
ECP		64	64										
ECP2		64	64										
ECP2M		64	64										
Sc		64											
MACHXO		64	64										
XP		64	64										
Xp2		64											

J32B_8B4

1 x 32-Bit input bus to 4 x 8-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Bus Joiner Resource Usage

J32B_8B4X

1 x 32-Bit IO bus to 4 x 8-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		64											
Cyclone		64	64										
Cyclone2		64	64										
Cyclone3		64	64										
Stratix		64	64										
Stratix2		64	64										
Stratix3		64											
StratixGX		64	64										
Stratix2gx		64											
Max2		64											
Max3000a	64	64											
Max7000b	64	64											
Max7000ae	64	64											
Max7000s	64	64											
Spartan2		64	64										
Spartan2E		64	64										
Spartan3		64	64										
Spartan3A		64											
Spartan3adsp		64											
Spartan3an		64											
Spartan3E		64	64										
Spartan3L		64	64										
Virtex		64	64										
Virtex2		64	64										
Virtex2p		64	64										
VirtexE		64	64										
Virtex4		64	64										
Virtex5		64	64										
ProAsicPlus		64	64										
ProAsic3		64	64										
ProAsic3E		64											
Fusion		64											
EC		64	64										
ECP		64	64										
ECP2		64	64										
ECP2M		64	64										
Sc		64											
MACHXO		64	64										
XP		64	64										
Xp2		64											

J32B_16B2

1 x 32-bit input bus to 2 x 16-Bit output bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Bus Joiner Resource Usage

J32B_16B2X

1 x 32-bit IO bus to 2 x 16-Bit IO bus

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		64											
Cyclone		64	64										
Cyclone2		64	64										
Cyclone3		64	64										
Stratix		64	64										
Stratix2		64	64										
Stratix3		64											
StratixGX		64	64										
Stratix2gx		64											
Max2		64											
Max3000a	64	64											
Max7000b	64	64											
Max7000ae	64	64											
Max7000s	64	64											
Spartan2		64	64										
Spartan2E		64	64										
Spartan3		64	64										
Spartan3A		64											
Spartan3adsp		64											
Spartan3an		64											
Spartan3E		64	64										
Spartan3L		64	64										
Virtex		64	64										
Virtex2		64	64										
Virtex2p		64	64										
VirtexE		64	64										
Virtex4		64	64										
Virtex5		64	64										
ProAsicPlus		64	64										
ProAsic3		64	64										
ProAsic3E		64											
Fusion		64											
EC		64	64										
ECP		64	64										
ECP2		64	64										
ECP2M		64	64										
Sc		64											
MACHXO		64	64										
XP		64	64										
Xp2		64											

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1

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