



FPGA Buffer Resource Usage

Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Buffer cores.

Core Reference
CR0125 (v1.11) December 19, 2008

Buffer

The available Buffer cores are listed as follows:

<i>BUF</i>	<i>BUF2B</i>	<i>BUF2S</i>	<i>BUF3B</i>
<i>BUF3S</i>	<i>BUF4B</i>	<i>BUF4S</i>	<i>BUF5B</i>
<i>BUF5S</i>	<i>BUF6B</i>	<i>BUF6S</i>	<i>BUF7B</i>
<i>BUF7S</i>	<i>BUF8B</i>	<i>BUF8S</i>	<i>BUF9B</i>
<i>BUF9S</i>	<i>BUF10B</i>	<i>BUF10S</i>	<i>BUF12B</i>
<i>BUF12S</i>	<i>BUF16B</i>	<i>BUF16S</i>	<i>BUF32B</i>
<i>BUF32S</i>	<i>BUFE</i>	<i>BUFE2B</i>	<i>BUFE2S</i>
<i>BUFE3B</i>	<i>BUFE3S</i>	<i>BUFE4B</i>	<i>BUFE4S</i>
<i>BUFE5B</i>	<i>BUFE5S</i>	<i>BUFE6B</i>	<i>BUFE6S</i>
<i>BUFE7B</i>	<i>BUFE7S</i>	<i>BUFE8B</i>	<i>BUFE8S</i>
<i>BUFE9B</i>	<i>BUFE9S</i>	<i>BUFE10B</i>	<i>BUFE10S</i>
<i>BUFE12B</i>	<i>BUFE12S</i>	<i>BUFE16B</i>	<i>BUFE16S</i>
<i>BUFE32B</i>	<i>BUFE32S</i>	<i>BUFT</i>	<i>BUFT2B</i>
<i>BUFT2S</i>	<i>BUFT3B</i>	<i>BUFT3S</i>	<i>BUFT4B</i>
<i>BUFT4S</i>	<i>BUFT5B</i>	<i>BUFT5S</i>	<i>BUFT6B</i>
<i>BUFT6S</i>	<i>BUFT7B</i>	<i>BUFT7S</i>	<i>BUFT8B</i>
<i>BUFT8S</i>	<i>BUFT9B</i>	<i>BUFT9S</i>	<i>BUFT10B</i>
<i>BUFT10S</i>	<i>BUFT12B</i>	<i>BUFT12S</i>	<i>BUFT16B</i>
<i>BUFT16S</i>	<i>BUFT32B</i>	<i>BUFT32S</i>	<i>IOBUF</i>
<i>IOBUF2B</i>	<i>IOBUF2S</i>	<i>IOBUF3B</i>	<i>IOBUF4B</i>
<i>IOBUF4S</i>	<i>IOBUF5B</i>	<i>IOBUF6B</i>	<i>IOBUF7B</i>
<i>IOBUF8B</i>	<i>IOBUF9B</i>	<i>IOBUF10B</i>	<i>IOBUF12B</i>
<i>IOBUF16B</i>	<i>IOBUF32B</i>	<i>IOBUFC2B</i>	<i>IOBUFC2S</i>
<i>IOBUFC3B</i>	<i>IOBUFC4B</i>	<i>IOBUFC4S</i>	<i>IOBUFC5B</i>
<i>IOBUFC6B</i>	<i>IOBUFC7B</i>	<i>IOBUFC8B</i>	<i>IOBUFC9B</i>
<i>IOBUFC10B</i>	<i>IOBUFC12B</i>	<i>IOBUFC16B</i>	<i>IOBUFC32B</i>

Legacy documentation
refer to the Altium Wiki for current information

FPGA Buffer Resource Usage

BUF

1-bit General Purpose (Non-inverting) Buffer

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		1											
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3		1											
StratixGX		1	1										
Stratix2gx		1											
Max2		1											
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1											
Spartan3adsp		1											
Spartan3an		1											
Spartan3E		1	1										
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		1	1										
Virtex5		1	1										
CoolRunner2	1	1											
CoolRunnerXpla3	1	1											
Xc9500	1	1											
Xc9500XL	1	1											
Xc9500XV	1	1											
ProAsicPlus		1	1										
ProAsic3		1	1										
ProAsic3E		1											
Fusion		1											
EC		1	1										
ECP		1	1										
ECP2		1	1										
ECP2M		1	1										
Sc		1											
MACHXO		1	1										
XP		1	1										
Xp2		1											

FPGA Buffer Resource Usage

BUF2B

2-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		2											
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3		2											
StratixGX		2	2										
Stratix2gx		2											
Max2		2											
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2											
Spartan3adsp		2											
Spartan3an		2											
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2	2										
CoolRunner2	2	2											
CoolRunnerXpla3	2	2											
Xc9500	2	2											
Xc9500XL	2	2											
Xc9500XV	2	2											
ProAsicPlus		2	2										
ProAsic3		2	2										
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
Sc		2											
MACHXO		2	2										
XP		2	2										
Xp2		2											

BUF2S

2-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		2											
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3		2											
StratixGX		2	2										
Stratix2gx		2											
Max2		2											
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2											
Spartan3adsp		2											
Spartan3an		2											
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2	2										
CoolRunner2	2	2											
CoolRunnerXpla3	2	2											
Xc9500	2	2											
Xc9500XL	2	2											
Xc9500XV	2	2											
ProAsicPlus		2	2										
ProAsic3		2	2										
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
Sc		2											
MACHXO		2	2										
XP		2	2										
Xp2		2											

FPGA Buffer Resource Usage

BUF3B

3-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		3											
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3		3											
StratixGX		3	3										
Stratix2gx		3											
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3											
Spartan3adsp		3											
Spartan3an		3											
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5		3	3										
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3	3										
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		3	3										
ECP2M		3	3										
Sc		3											
MACHXO		3	3										
XP		3	3										
Xp2		3											

BUF3S

3-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		3											
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3		3											
StratixGX		3	3										
Stratix2gx		3											
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3											
Spartan3adsp		3											
Spartan3an		3											
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5		3	3										
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3	3										
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		3	3										
ECP2M		3	3										
Sc		3											
MACHXO		3	3										
XP		3	3										
Xp2		3											

FPGA Buffer Resource Usage

BUF4B

4-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

BUF4S

4-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

FPGA Buffer Resource Usage

BUF5B

5-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		5											
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3		5											
StratixGX		5	5										
Stratix2gx		5											
Max2		5											
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A		5											
Spartan3adsp		5											
Spartan3an		5											
Spartan3E		5	5										
Spartan3L		5	5										
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5		5	5										
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5	5										
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		5	5										
ECP2M		5	5										
Sc		5											
MACHXO		5	5										
XP		5	5										
Xp2		5											

BUF5S

5-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		5											
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3		5											
StratixGX		5	5										
Stratix2gx		5											
Max2		5											
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A		5											
Spartan3adsp		5											
Spartan3an		5											
Spartan3E		5	5										
Spartan3L		5	5										
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5		5	5										
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5	5										
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		5	5										
ECP2M		5	5										
Sc		5											
MACHXO		5	5										
XP		5	5										
Xp2		5											

FPGA Buffer Resource Usage

BUF6B

6-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

BUF6S

6-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

FPGA Buffer Resource Usage

BUF7B

7-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7											
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3		7											
StratixGX		7	7										
Stratix2gx		7											
Max2		7											
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A		7											
Spartan3adsp		7											
Spartan3an		7											
Spartan3E		7	7										
Spartan3L		7	7										
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5		7	7										
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7	7										
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		7	7										
ECP2M		7	7										
Sc		7											
MACHXO		7	7										
XP		7	7										
Xp2		7											

BUF7S

7-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7											
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3		7											
StratixGX		7	7										
Stratix2gx		7											
Max2		7											
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A		7											
Spartan3adsp		7											
Spartan3an		7											
Spartan3E		7	7										
Spartan3L		7	7										
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5		7	7										
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7	7										
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		7	7										
ECP2M		7	7										
Sc		7											
MACHXO		7	7										
XP		7	7										
Xp2		7											

FPGA Buffer Resource Usage

BUF8B

8-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

BUF8S

8-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

FPGA Buffer Resource Usage

BUF9B

9-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		9											
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3		9											
StratixGX		9	9										
Stratix2gx		9											
Max2		9											
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A		9											
Spartan3adsp		9											
Spartan3an		9											
Spartan3E		9	9										
Spartan3L		9	9										
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5		9	9										
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9	9										
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		9	9										
ECP2M		9	9										
Sc		9											
MACHXO		9	9										
XP		9	9										
Xp2		9											

BUF9S

9-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		9											
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3		9											
StratixGX		9	9										
Stratix2gx		9											
Max2		9											
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A		9											
Spartan3adsp		9											
Spartan3an		9											
Spartan3E		9	9										
Spartan3L		9	9										
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5		9	9										
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9	9										
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		9	9										
ECP2M		9	9										
Sc		9											
MACHXO		9	9										
XP		9	9										
Xp2		9											

FPGA Buffer Resource Usage

BUF10B

10-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2	10	10											
CoolRunnerXpla3	10	10											
Xc9500	10	10											
Xc9500XL	10	10											
Xc9500XV	10	10											
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

BUF10S

10-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2	10	10											
CoolRunnerXpla3	10	10											
Xc9500	10	10											
Xc9500XL	10	10											
Xc9500XV	10	10											
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

FPGA Buffer Resource Usage

BUF12B

12-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

BUF12S

12-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

FPGA Buffer Resource Usage

BUF16B

16-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

BUF16S

16-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

FPGA Buffer Resource Usage

BUF32B

32-Bit General Purpose (Non-inverting) Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

BUF32S

32-Bit General Purpose (Non-inverting) Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Buffer Resource Usage

BUFE

1-bit 3-state Buffer with Active High Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		1											
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3		1											
StratixGX		1	1										
Stratix2gx		1											
Max2		1											
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1											
Spartan3adsp		1											
Spartan3an		1											
Spartan3E		1	1										
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		1	1										
Virtex5		1	1										
CoolRunner2	1	1											
CoolRunnerXpla3	1	1											
Xc9500	1	1											
Xc9500XL	1	1											
Xc9500XV	1	1											
ProAsicPlus		1	1										
ProAsic3		1	1										
ProAsic3E		1											
Fusion		1											
EC		1	1										
ECP		1	1										
ECP2		1	1										
ECP2M		1	1										
Sc		1											
MACHXO		1	1										
XP		1	1										
Xp2		1											

BUFE2B

2-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		2											
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3		2											
StratixGX		2	2										
Stratix2gx		2											
Max2		2											
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2											
Spartan3adsp		2											
Spartan3an		2											
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2	2										
CoolRunner2	2	2											
CoolRunnerXpla3	2	2											
Xc9500	2	2											
Xc9500XL	2	2											
Xc9500XV	2	2											
ProAsicPlus		2	2										
ProAsic3		2	2										
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
Sc		2											
MACHXO		2	2										
XP		2	2										
Xp2		2											

FPGA Buffer Resource Usage

BUFE2S

2-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		2											
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3		2											
StratixGX		2	2										
Stratix2gx		2											
Max2		2											
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2											
Spartan3adsp		2											
Spartan3an		2											
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2	2										
CoolRunner2	2	2											
CoolRunnerXpla3	2	2											
Xc9500	2	2											
Xc9500XL	2	2											
Xc9500XV	2	2											
ProAsicPlus		2	2										
ProAsic3		2	2										
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
Sc		2											
MACHXO		2	2										
XP		2	2										
Xp2		2											

BUFE3B

3-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		3											
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3		3											
StratixGX		3	3										
Stratix2gx		3											
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3											
Spartan3adsp		3											
Spartan3an		3											
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5		3	3										
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3	3										
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		3	3										
ECP2M		3	3										
Sc		3											
MACHXO		3	3										
XP		3	3										
Xp2		3											

FPGA Buffer Resource Usage

BUFE3S

3-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		3											
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3		3											
StratixGX		3	3										
Stratix2gx		3											
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3											
Spartan3adsp		3											
Spartan3an		3											
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5		3	3										
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3	3										
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		3	3										
ECP2M		3	3										
Sc		3											
MACHXO		3	3										
XP		3	3										
Xp2		3											

BUFE4B

4-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

FPGA Buffer Resource Usage

BUFE4S

4-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

BUFE5B

5-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		5											
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3		5	5										
StratixGX		5	5										
Stratix2gx		5											
Max2		5											
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A		5											
Spartan3adsp		5											
Spartan3an		5											
Spartan3E		5	5										
Spartan3L		5	5										
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5		5	5										
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5	5										
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		5	5										
ECP2M		5	5										
Sc		5											
MACHXO		5	5										
XP		5	5										
Xp2		5											

FPGA Buffer Resource Usage

BUFE5S

5-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		5											
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3		5											
StratixGX		5	5										
Stratix2gx		5											
Max2		5											
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A		5											
Spartan3adsp		5											
Spartan3an		5											
Spartan3E		5	5										
Spartan3L		5	5										
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5		5	5										
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5	5										
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		5	5										
ECP2M		5	5										
Sc		5											
MACHXO		5	5										
XP		5	5										
Xp2		5											

BUFE6B

6-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

FPGA Buffer Resource Usage

BUFE6S

6-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

BUFE7B

7-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7											
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3		7											
StratixGX		7	7										
Stratix2gx		7											
Max2		7											
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A		7											
Spartan3adsp		7											
Spartan3an		7											
Spartan3E		7	7										
Spartan3L		7	7										
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5		7	7										
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7	7										
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		7	7										
ECP2M		7	7										
Sc		7											
MACHXO		7	7										
XP		7	7										
Xp2		7											

FPGA Buffer Resource Usage

BUFE7S

7-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7											
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3		7											
StratixGX		7	7										
Stratix2gx		7											
Max2		7											
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A		7											
Spartan3adsp		7											
Spartan3an		7											
Spartan3E		7	7										
Spartan3L		7	7										
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5		7	7										
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7	7										
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		7	7										
ECP2M		7	7										
Sc		7											
MACHXO		7	7										
XP		7	7										
Xp2		7											

BUFE8B

8-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

FPGA Buffer Resource Usage

BUFE8S

8-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

BUFE9B

9-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		9											
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3		9											
StratixGX		9	9										
Stratix2gx		9											
Max2		9											
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A		9											
Spartan3adsp		9											
Spartan3an		9											
Spartan3E		9	9										
Spartan3L		9	9										
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5		9	9										
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9	9										
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		9	9										
ECP2M		9	9										
Sc		9											
MACHXO		9	9										
XP		9	9										
Xp2		9											

FPGA Buffer Resource Usage

BUFE9S

9-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		9											
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3		9											
StratixGX		9	9										
Stratix2gx		9											
Max2		9											
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A		9											
Spartan3adsp		9											
Spartan3an		9											
Spartan3E		9	9										
Spartan3L		9	9										
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5		9	9										
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9	9										
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		9	9										
ECP2M		9	9										
Sc		9											
MACHXO		9	9										
XP		9	9										
Xp2		9											

BUFE10B

10-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2	10	10											
CoolRunnerXpla3	10	10											
Xc9500	10	10											
Xc9500XL	10	10											
Xc9500XV	10	10											
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

FPGA Buffer Resource Usage

BUFE10S

10-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2	10	10											
CoolRunnerXpla3	10	10											
Xc9500	10	10											
Xc9500XL	10	10											
Xc9500XV	10	10											
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

BUFE12B

12-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

FPGA Buffer Resource Usage

BUFE12S

12-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

BUFE16B

16-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

FPGA Buffer Resource Usage

BUFE16S

16-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

BUFE32B

32-Bit 3-state Buffer with Active High Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Buffer Resource Usage

BUFE32S

32-Bit 3-state Buffer with Active High Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

BUFT

1-Bit 3-state Buffer with Active Low Enable

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		1											
Cyclone		1	1										
Cyclone2		1	1										
Cyclone3		1	1										
Stratix		1	1										
Stratix2		1	1										
Stratix3		1											
StratixGX		1	1										
Stratix2gx		1											
Max2		1											
Max3000a	1	1											
Max7000b	1	1											
Max7000ae	1	1											
Max7000s	1	1											
Spartan2		1	1										
Spartan2E		1	1										
Spartan3		1	1										
Spartan3A		1											
Spartan3adsp		1											
Spartan3an		1											
Spartan3E		1	1										
Spartan3L		1	1										
Virtex		1	1										
Virtex2		1	1										
Virtex2p		1	1										
VirtexE		1	1										
Virtex4		1	1										
Virtex5		1	1										
CoolRunner2	1	1											
CoolRunnerXpla3	1	1											
Xc9500	1	1											
Xc9500XL	1	1											
Xc9500XV	1	1											
ProAsicPlus		1	1										
ProAsic3		1	1										
ProAsic3E		1											
Fusion		1											
EC		1	1										
ECP		1	1										
ECP2		1	1										
ECP2M		1	1										
Sc		1											
MACHXO		1	1										
XP		1	1										
Xp2		1											

FPGA Buffer Resource Usage

BUFT2B

2-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		2											
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3		2											
StratixGX		2	2										
Stratix2gx		2											
Max2		2											
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2											
Spartan3adsp		2											
Spartan3an		2											
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2	2										
CoolRunner2	2	2											
CoolRunnerXpla3	2	2											
Xc9500	2	2											
Xc9500XL	2	2											
Xc9500XV	2	2											
ProAsicPlus		2	2										
ProAsic3		2	2										
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
Sc		2											
MACHXO		2	2										
XP		2	2										
Xp2		2											

BUFT2S

2-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		2											
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3		2											
StratixGX		2	2										
Stratix2gx		2											
Max2		2											
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2											
Spartan3adsp		2											
Spartan3an		2											
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2	2										
CoolRunner2	2	2											
CoolRunnerXpla3	2	2											
Xc9500	2	2											
Xc9500XL	2	2											
Xc9500XV	2	2											
ProAsicPlus		2	2										
ProAsic3		2	2										
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
Sc		2											
MACHXO		2	2										
XP		2	2										
Xp2		2											

FPGA Buffer Resource Usage

BUFT3B

3-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		3											
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3		3											
StratixGX		3	3										
Stratix2gx		3											
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3											
Spartan3adsp		3											
Spartan3an		3											
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5		3	3										
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3	3										
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		3	3										
ECP2M		3	3										
Sc		3											
MACHXO		3	3										
XP		3	3										
Xp2		3											

BUFT3S

3-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		3											
Cyclone		3	3										
Cyclone2		3	3										
Cyclone3		3	3										
Stratix		3	3										
Stratix2		3	3										
Stratix3		3											
StratixGX		3	3										
Stratix2gx		3											
Max2		3											
Max3000a	3	3											
Max7000b	3	3											
Max7000ae	3	3											
Max7000s	3	3											
Spartan2		3	3										
Spartan2E		3	3										
Spartan3		3	3										
Spartan3A		3											
Spartan3adsp		3											
Spartan3an		3											
Spartan3E		3	3										
Spartan3L		3	3										
Virtex		3	3										
Virtex2		3	3										
Virtex2p		3	3										
VirtexE		3	3										
Virtex4		3	3										
Virtex5		3	3										
CoolRunner2	3	3											
CoolRunnerXpla3	3	3											
Xc9500	3	3											
Xc9500XL	3	3											
Xc9500XV	3	3											
ProAsicPlus		3	3										
ProAsic3		3	3										
ProAsic3E		3											
Fusion		3											
EC		3	3										
ECP		3	3										
ECP2		3	3										
ECP2M		3	3										
Sc		3											
MACHXO		3	3										
XP		3	3										
Xp2		3											

FPGA Buffer Resource Usage

BUFT4B

4-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

BUFT4S

4-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

FPGA Buffer Resource Usage

BUFT5B

5-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		5											
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3		5											
StratixGX		5	5										
Stratix2gx		5											
Max2		5											
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A		5											
Spartan3adsp		5											
Spartan3an		5											
Spartan3E		5	5										
Spartan3L		5	5										
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5		5	5										
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5	5										
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		5	5										
ECP2M		5	5										
Sc		5											
MACHXO		5	5										
XP		5	5										
Xp2		5											

BUFT5S

5-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		5											
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		5	5										
Stratix3		5											
StratixGX		5	5										
Stratix2gx		5											
Max2		5											
Max3000a	5	5											
Max7000b	5	5											
Max7000ae	5	5											
Max7000s	5	5											
Spartan2		5	5										
Spartan2E		5	5										
Spartan3		5	5										
Spartan3A		5											
Spartan3adsp		5											
Spartan3an		5											
Spartan3E		5	5										
Spartan3L		5	5										
Virtex		5	5										
Virtex2		5	5										
Virtex2p		5	5										
VirtexE		5	5										
Virtex4		5	5										
Virtex5		5	5										
CoolRunner2	5	5											
CoolRunnerXpla3	5	5											
Xc9500	5	5											
Xc9500XL	5	5											
Xc9500XV	5	5											
ProAsicPlus		5	5										
ProAsic3		5	5										
ProAsic3E		5											
Fusion		5											
EC		5	5										
ECP		5	5										
ECP2		5	5										
ECP2M		5	5										
Sc		5											
MACHXO		5	5										
XP		5	5										
Xp2		5											

FPGA Buffer Resource Usage

BUFT6B

6-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

BUFT6S

6-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

FPGA Buffer Resource Usage

BUFT7B

7-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7											
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3		7											
StratixGX		7	7										
Stratix2gx		7											
Max2		7											
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A		7											
Spartan3adsp		7											
Spartan3an		7											
Spartan3E		7	7										
Spartan3L		7	7										
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5		7	7										
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7	7										
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		7	7										
ECP2M		7	7										
Sc		7											
MACHXO		7	7										
XP		7	7										
Xp2		7											

BUFT7S

7-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		7											
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3		7											
StratixGX		7	7										
Stratix2gx		7											
Max2		7											
Max3000a	7	7											
Max7000b	7	7											
Max7000ae	7	7											
Max7000s	7	7											
Spartan2		7	7										
Spartan2E		7	7										
Spartan3		7	7										
Spartan3A		7											
Spartan3adsp		7											
Spartan3an		7											
Spartan3E		7	7										
Spartan3L		7	7										
Virtex		7	7										
Virtex2		7	7										
Virtex2p		7	7										
VirtexE		7	7										
Virtex4		7	7										
Virtex5		7	7										
CoolRunner2	7	7											
CoolRunnerXpla3	7	7											
Xc9500	7	7											
Xc9500XL	7	7											
Xc9500XV	7	7											
ProAsicPlus		7	7										
ProAsic3		7	7										
ProAsic3E		7											
Fusion		7											
EC		7	7										
ECP		7	7										
ECP2		7	7										
ECP2M		7	7										
Sc		7											
MACHXO		7	7										
XP		7	7										
Xp2		7											

FPGA Buffer Resource Usage

BUFT8B

8-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

BUFT8S

8-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

FPGA Buffer Resource Usage

BUFT9B

9-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		9											
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3		9											
StratixGX		9	9										
Stratix2gx		9											
Max2		9											
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A		9											
Spartan3adsp		9											
Spartan3an		9											
Spartan3E		9	9										
Spartan3L		9	9										
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5		9	9										
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9	9										
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		9	9										
ECP2M		9	9										
Sc		9											
MACHXO		9	9										
XP		9	9										
Xp2		9											

BUFT9S

9-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		9											
Cyclone		9	9										
Cyclone2		9	9										
Cyclone3		9	9										
Stratix		9	9										
Stratix2		9	9										
Stratix3		9											
StratixGX		9	9										
Stratix2gx		9											
Max2		9											
Max3000a	9	9											
Max7000b	9	9											
Max7000ae	9	9											
Max7000s	9	9											
Spartan2		9	9										
Spartan2E		9	9										
Spartan3		9	9										
Spartan3A		9											
Spartan3adsp		9											
Spartan3an		9											
Spartan3E		9	9										
Spartan3L		9	9										
Virtex		9	9										
Virtex2		9	9										
Virtex2p		9	9										
VirtexE		9	9										
Virtex4		9	9										
Virtex5		9	9										
CoolRunner2	9	9											
CoolRunnerXpla3	9	9											
Xc9500	9	9											
Xc9500XL	9	9											
Xc9500XV	9	9											
ProAsicPlus		9	9										
ProAsic3		9	9										
ProAsic3E		9											
Fusion		9											
EC		9	9										
ECP		9	9										
ECP2		9	9										
ECP2M		9	9										
Sc		9											
MACHXO		9	9										
XP		9	9										
Xp2		9											

FPGA Buffer Resource Usage

BUFT10B

10-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2	10	10											
CoolRunnerXpla3	10	10											
Xc9500	10	10											
Xc9500XL	10	10											
Xc9500XV	10	10											
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

BUFT10S

10-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2	10	10											
CoolRunnerXpla3	10	10											
Xc9500	10	10											
Xc9500XL	10	10											
Xc9500XV	10	10											
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

FPGA Buffer Resource Usage

BUFT12B

12-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

BUFT12S

12-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

FPGA Buffer Resource Usage

BUFT16B

16-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

BUFT16S

16-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

FPGA Buffer Resource Usage

BUFT32B

32-Bit 3-state Buffer with Active Low Enable, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

BUFT32S

32-Bit 3-state Buffer with Active Low Enable, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Buffer Resource Usage

IOBUF

Input/Output Buffer

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		2											
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3		2											
StratixGX		2	2										
Stratix2gx		2											
Max2		2											
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2											
Spartan3adsp		2											
Spartan3an		2											
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2	2										
CoolRunner2	2	2											
CoolRunnerXpla3	2	2											
Xc9500	2	2											
Xc9500XL	2	2											
Xc9500XV	2	2											
ProAsicPlus		2	2										
ProAsic3		2	2										
ProAsic3E		2											
Fusion		2											
EC		2	2										
ECP		2	2										
ECP2		2	2										
ECP2M		2	2										
Sc		2											
MACHXO		2	2										
XP		2	2										
Xp2		2											

IOBUF2B

2-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

FPGA Buffer Resource Usage

IOBUF2S

2-Bit Input/Output Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

IOBUF3B

3-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

FPGA Buffer Resource Usage

IOBUF4B

4-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

IOBUF4S

4-Bit Input/Output Buffer, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

FPGA Buffer Resource Usage

IOBUF5B

5-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2	10	10											
CoolRunnerXpla3	10	10											
Xc9500	10	10											
Xc9500XL	10	10											
Xc9500XV	10	10											
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

IOBUF6B

6-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

FPGA Buffer Resource Usage

IOBUF7B

7-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		14											
Cyclone		14	14										
Cyclone2		14	14										
Cyclone3		14	14										
Stratix		14	14										
Stratix2		14	14										
Stratix3		14											
StratixGX		14	14										
Stratix2gx		14											
Max2		14											
Max3000a	14	14											
Max7000b	14	14											
Max7000ae	14	14											
Max7000s	14	14											
Spartan2		14	14										
Spartan2E		14	14										
Spartan3		14	14										
Spartan3A		14											
Spartan3adsp		14											
Spartan3an		14											
Spartan3E		14	14										
Spartan3L		14	14										
Virtex		14	14										
Virtex2		14	14										
Virtex2p		14	14										
VirtexE		14	14										
Virtex4		14	14										
Virtex5		14	14										
CoolRunner2	14	14											
CoolRunnerXpla3	14	14											
Xc9500	14	14											
Xc9500XL	14	14											
Xc9500XV	14	14											
ProAsicPlus		14	14										
ProAsic3		14	14										
ProAsic3E		14											
Fusion		14											
EC		14	14										
ECP		14	14										
ECP2		14	14										
ECP2M		14	14										
Sc		14											
MACHXO		14	14										
XP		14	14										
Xp2		14											

IOBUF8B

8-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

FPGA Buffer Resource Usage

IOBUF9B

9-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		18											
Cyclone		18	18										
Cyclone2		18	18										
Cyclone3		18	18										
Stratix		18	18										
Stratix2		18	18										
Stratix3		18											
StratixGX		18	18										
Stratix2gx		18											
Max2		18											
Max3000a	18	18											
Max7000b	18	18											
Max7000ae	18	18											
Max7000s	18	18											
Spartan2		18	18										
Spartan2E		18	18										
Spartan3		18	18										
Spartan3A		18											
Spartan3adsp		18											
Spartan3an		18											
Spartan3E		18	18										
Spartan3L		18	18										
Virtex		18	18										
Virtex2		18	18										
Virtex2p		18	18										
VirtexE		18	18										
Virtex4		18	18										
Virtex5		18	18										
CoolRunner2	18	18											
CoolRunnerXpla3	18	18											
Xc9500	18	18											
Xc9500XL	18	18											
Xc9500XV	18	18											
ProAsicPlus		18	18										
ProAsic3		18	18										
ProAsic3E		18											
Fusion		18											
EC		18	18										
ECP		18	18										
ECP2		18	18										
ECP2M		18	18										
Sc		18											
MACHXO		18	18										
XP		18	18										
Xp2		18											

IOBUF10B

10-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		20											
Cyclone		20	20										
Cyclone2		20	20										
Cyclone3		20	20										
Stratix		20	20										
Stratix2		20	20										
Stratix3		20											
StratixGX		20	20										
Stratix2gx		20											
Max2		20											
Max3000a	20	20											
Max7000b	20	20											
Max7000ae	20	20											
Max7000s	20	20											
Spartan2		20	20										
Spartan2E		20	20										
Spartan3		20	20										
Spartan3A		20											
Spartan3adsp		20											
Spartan3an		20											
Spartan3E		20	20										
Spartan3L		20	20										
Virtex		20	20										
Virtex2		20	20										
Virtex2p		20	20										
VirtexE		20	20										
Virtex4		20	20										
Virtex5		20	20										
CoolRunner2	20	20											
CoolRunnerXpla3	20	20											
Xc9500	20	20											
Xc9500XL	20	20											
Xc9500XV	20	20											
ProAsicPlus		20	20										
ProAsic3		20	20										
ProAsic3E		20											
Fusion		20											
EC		20	20										
ECP		20	20										
ECP2		20	20										
ECP2M		20	20										
Sc		20											
MACHXO		20	20										
XP		20	20										
Xp2		20											

FPGA Buffer Resource Usage

IOBUF12B

12-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		24											
Cyclone		24	24										
Cyclone2		24	24										
Cyclone3		24	24										
Stratix		24	24										
Stratix2		24	24										
Stratix3		24											
StratixGX		24	24										
Stratix2gx		24											
Max2		24											
Max3000a	24	24											
Max7000b	24	24											
Max7000ae	24	24											
Max7000s	24	24											
Spartan2		24	24										
Spartan2E		24	24										
Spartan3		24	24										
Spartan3A		24											
Spartan3adsp		24											
Spartan3an		24											
Spartan3E		24	24										
Spartan3L		24	24										
Virtex		24	24										
Virtex2		24	24										
Virtex2p		24	24										
VirtexE		24	24										
Virtex4		24	24										
Virtex5		24	24										
CoolRunner2	24	24											
CoolRunnerXpla3	24	24											
Xc9500	24	24											
Xc9500XL	24	24											
Xc9500XV	24	24											
ProAsicPlus		24	24										
ProAsic3		24	24										
ProAsic3E		24											
Fusion		24											
EC		24	24										
ECP		24	24										
ECP2		24	24										
ECP2M		24	24										
Sc		24											
MACHXO		24	24										
XP		24	24										
Xp2		24											

IOBUF16B

16-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Buffer Resource Usage

IOBUF32B

32-Bit Input/Output Buffer, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		64											
Cyclone		64	64										
Cyclone2		64	64										
Cyclone3		64	64										
Stratix		64	64										
Stratix2		64	64										
Stratix3		64											
StratixGX		64	64										
Stratix2gx		64											
Max2		64											
Max3000a	64	64											
Max7000b	64	64											
Max7000ae	64	64											
Max7000s	64	64											
Spartan2		64	64										
Spartan2E		64	64										
Spartan3		64	64										
Spartan3A		64											
Spartan3adsp		64											
Spartan3an		64											
Spartan3E		64	64										
Spartan3L		64	64										
Virtex		64	64										
Virtex2		64	64										
Virtex2p		64	64										
VirtexE		64	64										
Virtex4		64	64										
Virtex5		64	64										
CoolRunner2	64	64											
CoolRunnerXpla3	64	64											
Xc9500	64	64											
Xc9500XL	64	64											
Xc9500XV	64	64											
ProAsicPlus		64	64										
ProAsic3		64	64										
ProAsic3E		64											
Fusion		64											
EC		64	64										
ECP		64	64										
ECP2		64	64										
ECP2M		64	64										
Sc		64											
MACHXO		64	64										
XP		64	64										
Xp2		64											

IOBUFC2B

2-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

FPGA Buffer Resource Usage

IOBUFC2S

2-Bit Input/Output Buffer With Separated Control, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		4											
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3		4											
StratixGX		4	4										
Stratix2gx		4											
Max2		4											
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		4	4										
Spartan3A		4											
Spartan3adsp		4											
Spartan3an		4											
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		4	4										
Virtex2p		4	4										
VirtexE		4	4										
Virtex4		4	4										
Virtex5		4	4										
CoolRunner2	4	4											
CoolRunnerXpla3	4	4											
Xc9500	4	4											
Xc9500XL	4	4											
Xc9500XV	4	4											
ProAsicPlus		4	4										
ProAsic3		4	4										
ProAsic3E		4											
Fusion		4											
EC		4	4										
ECP		4	4										
ECP2		4	4										
ECP2M		4	4										
Sc		4											
MACHXO		4	4										
XP		4	4										
Xp2		4											

IOBUFC3B

3-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6											
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3		6											
StratixGX		6	6										
Stratix2gx		6											
Max2		6											
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	6										
Spartan2E		6	6										
Spartan3		6	6										
Spartan3A		6											
Spartan3adsp		6											
Spartan3an		6											
Spartan3E		6	6										
Spartan3L		6	6										
Virtex		6	6										
Virtex2		6	6										
Virtex2p		6	6										
VirtexE		6	6										
Virtex4		6	6										
Virtex5		6	6										
CoolRunner2	6	6											
CoolRunnerXpla3	6	6											
Xc9500	6	6											
Xc9500XL	6	6											
Xc9500XV	6	6											
ProAsicPlus		6	6										
ProAsic3		6	6										
ProAsic3E		6											
Fusion		6											
EC		6	6										
ECP		6	6										
ECP2		6	6										
ECP2M		6	6										
Sc		6											
MACHXO		6	6										
XP		6	6										
Xp2		6											

FPGA Buffer Resource Usage

IOBUFC4B

4-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

IOBUFC4S

4-Bit Input/Output Buffer With Separated Control, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		8											
Cyclone		8	8										
Cyclone2		8	8										
Cyclone3		8	8										
Stratix		8	8										
Stratix2		8	8										
Stratix3		8											
StratixGX		8	8										
Stratix2gx		8											
Max2		8											
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8											
Spartan3adsp		8											
Spartan3an		8											
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5		8	8										
CoolRunner2	8	8											
CoolRunnerXpla3	8	8											
Xc9500	8	8											
Xc9500XL	8	8											
Xc9500XV	8	8											
ProAsicPlus		8	8										
ProAsic3		8	8										
ProAsic3E		8											
Fusion		8											
EC		8	8										
ECP		8	8										
ECP2		8	8										
ECP2M		8	8										
Sc		8											
MACHXO		8	8										
XP		8	8										
Xp2		8											

FPGA Buffer Resource Usage

IOBUFC5B

5-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		10											
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3		10											
StratixGX		10	10										
Stratix2gx		10											
Max2		10											
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		10	10										
Spartan3A		10											
Spartan3adsp		10											
Spartan3an		10											
Spartan3E		10	10										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		10	10										
Virtex2p		10	10										
VirtexE		10	10										
Virtex4		10	10										
Virtex5		10	10										
CoolRunner2	10	10											
CoolRunnerXpla3	10	10											
Xc9500	10	10											
Xc9500XL	10	10											
Xc9500XV	10	10											
ProAsicPlus		10	10										
ProAsic3		10	10										
ProAsic3E		10											
Fusion		10											
EC		10	10										
ECP		10	10										
ECP2		10	10										
ECP2M		10	10										
Sc		10											
MACHXO		10	10										
XP		10	10										
Xp2		10											

IOBUFC6B

6-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		12											
Cyclone		12	12										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		12	12										
Stratix2		12	12										
Stratix3		12											
StratixGX		12	12										
Stratix2gx		12											
Max2		12											
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		12	12										
Spartan3A		12											
Spartan3adsp		12											
Spartan3an		12											
Spartan3E		12	12										
Spartan3L		12	12										
Virtex		12	12										
Virtex2		12	12										
Virtex2p		12	12										
VirtexE		12	12										
Virtex4		12	12										
Virtex5		12	12										
CoolRunner2	12	12											
CoolRunnerXpla3	12	12											
Xc9500	12	12											
Xc9500XL	12	12											
Xc9500XV	12	12											
ProAsicPlus		12	12										
ProAsic3		12	12										
ProAsic3E		12											
Fusion		12											
EC		12	12										
ECP		12	12										
ECP2		12	12										
ECP2M		12	12										
Sc		12											
MACHXO		12	12										
XP		12	12										
Xp2		12											

FPGA Buffer Resource Usage

IOBUFC7B

7-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		14											
Cyclone		14	14										
Cyclone2		14	14										
Cyclone3		14	14										
Stratix		14	14										
Stratix2		14	14										
Stratix3		14											
StratixGX		14	14										
Stratix2gx		14											
Max2		14											
Max3000a	14	14											
Max7000b	14	14											
Max7000ae	14	14											
Max7000s	14	14											
Spartan2		14	14										
Spartan2E		14	14										
Spartan3		14	14										
Spartan3A		14											
Spartan3adsp		14											
Spartan3an		14											
Spartan3E		14	14										
Spartan3L		14	14										
Virtex		14	14										
Virtex2		14	14										
Virtex2p		14	14										
VirtexE		14	14										
Virtex4		14	14										
Virtex5		14	14										
CoolRunner2	14	14											
CoolRunnerXpla3	14	14											
Xc9500	14	14											
Xc9500XL	14	14											
Xc9500XV	14	14											
ProAsicPlus		14	14										
ProAsic3		14	14										
ProAsic3E		14											
Fusion		14											
EC		14	14										
ECP		14	14										
ECP2		14	14										
ECP2M		14	14										
Sc		14											
MACHXO		14	14										
XP		14	14										
Xp2		14											

IOBUFC8B

8-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		16											
Cyclone		16	16										
Cyclone2		16	16										
Cyclone3		16	16										
Stratix		16	16										
Stratix2		16	16										
Stratix3		16											
StratixGX		16	16										
Stratix2gx		16											
Max2		16											
Max3000a	16	16											
Max7000b	16	16											
Max7000ae	16	16											
Max7000s	16	16											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16											
Spartan3adsp		16											
Spartan3an		16											
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		16	16										
CoolRunner2	16	16											
CoolRunnerXpla3	16	16											
Xc9500	16	16											
Xc9500XL	16	16											
Xc9500XV	16	16											
ProAsicPlus		16	16										
ProAsic3		16	16										
ProAsic3E		16											
Fusion		16											
EC		16	16										
ECP		16	16										
ECP2		16	16										
ECP2M		16	16										
Sc		16											
MACHXO		16	16										
XP		16	16										
Xp2		16											

FPGA Buffer Resource Usage

IOBUFC9B

9-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		18											
Cyclone		18	18										
Cyclone2		18	18										
Cyclone3		18	18										
Stratix		18	18										
Stratix2		18	18										
Stratix3		18											
StratixGX		18	18										
Stratix2gx		18											
Max2		18											
Max3000a	18	18											
Max7000b	18	18											
Max7000ae	18	18											
Max7000s	18	18											
Spartan2		18	18										
Spartan2E		18	18										
Spartan3		18	18										
Spartan3A		18											
Spartan3adsp		18											
Spartan3an		18											
Spartan3E		18	18										
Spartan3L		18	18										
Virtex		18	18										
Virtex2		18	18										
Virtex2p		18	18										
VirtexE		18	18										
Virtex4		18	18										
Virtex5		18	18										
CoolRunner2	18	18											
CoolRunnerXpla3	18	18											
Xc9500	18	18											
Xc9500XL	18	18											
Xc9500XV	18	18											
ProAsicPlus		18	18										
ProAsic3		18	18										
ProAsic3E		18											
Fusion		18											
EC		18	18										
ECP		18	18										
ECP2		18	18										
ECP2M		18	18										
Sc		18											
MACHXO		18	18										
XP		18	18										
Xp2		18											

IOBUFC10B

10-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		20											
Cyclone		20	20										
Cyclone2		20	20										
Cyclone3		20	20										
Stratix		20	20										
Stratix2		20	20										
Stratix3		20											
StratixGX		20	20										
Stratix2gx		20											
Max2		20											
Max3000a	20	20											
Max7000b	20	20											
Max7000ae	20	20											
Max7000s	20	20											
Spartan2		20	20										
Spartan2E		20	20										
Spartan3		20	20										
Spartan3A		20											
Spartan3adsp		20											
Spartan3an		20											
Spartan3E		20	20										
Spartan3L		20	20										
Virtex		20	20										
Virtex2		20	20										
Virtex2p		20	20										
VirtexE		20	20										
Virtex4		20	20										
Virtex5		20	20										
CoolRunner2	20	20											
CoolRunnerXpla3	20	20											
Xc9500	20	20											
Xc9500XL	20	20											
Xc9500XV	20	20											
ProAsicPlus		20	20										
ProAsic3		20	20										
ProAsic3E		20											
Fusion		20											
EC		20	20										
ECP		20	20										
ECP2		20	20										
ECP2M		20	20										
Sc		20											
MACHXO		20	20										
XP		20	20										
Xp2		20											

FPGA Buffer Resource Usage

IOBUFC12B

12-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		24											
Cyclone		24	24										
Cyclone2		24	24										
Cyclone3		24	24										
Stratix		24	24										
Stratix2		24	24										
Stratix3		24											
StratixGX		24	24										
Stratix2gx		24											
Max2		24											
Max3000a	24	24											
Max7000b	24	24											
Max7000ae	24	24											
Max7000s	24	24											
Spartan2		24	24										
Spartan2E		24	24										
Spartan3		24	24										
Spartan3A		24											
Spartan3adsp		24											
Spartan3an		24											
Spartan3E		24	24										
Spartan3L		24	24										
Virtex		24	24										
Virtex2		24	24										
Virtex2p		24	24										
VirtexE		24	24										
Virtex4		24	24										
Virtex5		24	24										
CoolRunner2	24	24											
CoolRunnerXpla3	24	24											
Xc9500	24	24											
Xc9500XL	24	24											
Xc9500XV	24	24											
ProAsicPlus		24	24										
ProAsic3		24	24										
ProAsic3E		24											
Fusion		24											
EC		24	24										
ECP		24	24										
ECP2		24	24										
ECP2M		24	24										
Sc		24											
MACHXO		24	24										
XP		24	24										
Xp2		24											

IOBUFC16B

16-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		32											
Cyclone		32	32										
Cyclone2		32	32										
Cyclone3		32	32										
Stratix		32	32										
Stratix2		32	32										
Stratix3		32											
StratixGX		32	32										
Stratix2gx		32											
Max2		32											
Max3000a	32	32											
Max7000b	32	32											
Max7000ae	32	32											
Max7000s	32	32											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32											
Spartan3adsp		32											
Spartan3an		32											
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		32	32										
CoolRunner2	32	32											
CoolRunnerXpla3	32	32											
Xc9500	32	32											
Xc9500XL	32	32											
Xc9500XV	32	32											
ProAsicPlus		32	32										
ProAsic3		32	32										
ProAsic3E		32											
Fusion		32											
EC		32	32										
ECP		32	32										
ECP2		32	32										
ECP2M		32	32										
Sc		32											
MACHXO		32	32										
XP		32	32										
Xp2		32											

FPGA Buffer Resource Usage

IOBUFC32B

32-Bit Input/Output Buffer With Separated Control, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		64											
Cyclone		64	64										
Cyclone2		64	64										
Cyclone3		64	64										
Stratix		64	64										
Stratix2		64	64										
Stratix3		64											
StratixGX		64	64										
Stratix2gx		64											
Max2		64											
Max3000a	64	64											
Max7000b	64	64											
Max7000ae	64	64											
Max7000s	64	64											
Spartan2		64	64										
Spartan2E		64	64										
Spartan3		64	64										
Spartan3A		64											
Spartan3adsp		64											
Spartan3an		64											
Spartan3E		64	64										
Spartan3L		64	64										
Virtex		64	64										
Virtex2		64	64										
Virtex2p		64	64										
VirtexE		64	64										
Virtex4		64	64										
Virtex5		64	64										
CoolRunner2	64	64											
CoolRunnerXpla3	64	64											
Xc9500	64	64											
Xc9500XL	64	64											
Xc9500XV	64	64											
ProAsicPlus		64	64										
ProAsic3		64	64										
ProAsic3E		64											
Fusion		64											
EC		64	64										
ECP		64	64										
ECP2		64	64										
ECP2M		64	64										
Sc		64											
MACHXO		64	64										
XP		64	64										
Xp2		64											

Tools Utilized

The following vendor device tools were used to determine the resource usage statistics:

Actel

Actel Designer Software Version 6.2

Altera

Quartus II 5.0

Lattice

ispLEVER 5.0

Xilinx

Xilinx ISE 6.3

For Virtex4, Spartan3, Spartan3E the Xilinx ISE 7.1 was used.

Revision History

Date	Version No.	Revision
6-Dec-2004	1.0	Service pack 2 release
12-Apr-2005	1.01	Added Virtex4 and Stratix2 resource usage
6-Jun-2005	1.02	Added MAX2 resource usage
15-Sep-2005	1.03	Added EC, ECP, Spartan3E, Cyclone2 and StratixGX resource usage
13-Oct-2005	1.04	Added ProAsic3 and ProAsic3E resource usage
20-Apr-2006	1.06	Tools Utilized section added
16-Jun-2006	1.07	XP resource usage added
28-Jul-2006	1.08	MACHXO resource usage added
10-Apr-2007	1.09	Cyclone3, ECP2, ECP2M, Spartan3A, Spartan3E, Spartan3L and Virtex5 resource usage added
17-Jul-2008	1.10	Altium Designer Summer 08 SP1
19-Dec-2008	1.11	Altium Designer Winter 09 SP1

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