



## FPGA Arithmetic Function Resource Usage

### Summary

This quick reference provides detailed information about resource usage of all pre-synthesized Arithmetic Function cores.

Core Reference  
CR0124 (v1.11) December 19, 2008

### Arithmetic Function

The available Arithmetic Function cores are listed as follows:

<i>ACC1</i>	<i>ACC2B</i>	<i>ACC2S</i>	<i>ACC4B</i>
<i>ACC4S</i>	<i>ACC8B</i>	<i>ACC16B</i>	<i>ACC32B</i>
<i>ADD1</i>	<i>ADD2B</i>	<i>ADD2S</i>	<i>ADD4B</i>
<i>ADD4S</i>	<i>ADD8B</i>	<i>ADD16B</i>	<i>ADD32B</i>
<i>ADDF2B</i>	<i>ADDF2S</i>	<i>ADDF4B</i>	<i>ADDF4S</i>
<i>ADDF8B</i>	<i>ADDF16B</i>	<i>ADDF32B</i>	<i>ADDFR2B</i>
<i>ADDFR2S</i>	<i>ADDFR4B</i>	<i>ADDFR4S</i>	<i>ADDFR8B</i>
<i>ADDFR16B</i>	<i>ADDFR32B</i>	<i>ADDR1</i>	<i>ADDR2B</i>
<i>ADDR2S</i>	<i>ADDR4B</i>	<i>ADDR4S</i>	<i>ADDR8B</i>
<i>ADDR16B</i>	<i>ADDR32B</i>	<i>ADSU1</i>	<i>ADSU2B</i>
<i>ADSU2S</i>	<i>ADSU4B</i>	<i>ADSU4S</i>	<i>ADSU8B</i>
<i>ADSU16B</i>	<i>ADSU32B</i>	<i>ADSUR1</i>	<i>ADSUR2B</i>
<i>ADSUR2S</i>	<i>ADSUR4B</i>	<i>ADSUR4S</i>	<i>ADSUR8B</i>
<i>ADSUR16B</i>	<i>ADSUR32B</i>	<i>MULT2B</i>	<i>MULT2S</i>
<i>MULT4B</i>	<i>MULT4S</i>	<i>MULT8B</i>	<i>MULT16B</i>
<i>MULT18B</i>	<i>MULT32B</i>	<i>MULTR2B</i>	<i>MULTR2S</i>
<i>MULTR4B</i>	<i>MULTR4S</i>	<i>MULTR8B</i>	<i>MULTR16B</i>
<i>MULTR18B</i>	<i>MULTR32B</i>	<i>MULTU2B</i>	<i>MULTU2S</i>
<i>MULTU4B</i>	<i>MULTU4S</i>	<i>MULTU8B</i>	<i>MULTU16B</i>
<i>MULTU18B</i>	<i>MULTU32B</i>	<i>MULTUR2B</i>	<i>MULTUR2S</i>
<i>MULTUR4B</i>	<i>MULTUR4S</i>	<i>MULTUR8B</i>	<i>MULTUR16B</i>
<i>MULTUR18B</i>	<i>MULTUR32B</i>	<i>PAR9B</i>	<i>PAR9S</i>

**FPGA Arithmetic Function Resource Usage**

**ACC1**

**1-Bit Loadable Cascadable Accumulator with Synchronous Reset**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	1									
Cyclone		4	4	1									
Cyclone2		4	4	1									
Cyclone3		4	4	1									
Stratix		4	4	1									
Stratix2		6	6	1									
Stratix3			3	1									
StratixGX		4	4	1									
Stratix2GX			3	1									
Max2		4	4	1									
Max3000a	3	3		1									
Max7000b	3	3		1									
Max7000ae	3	3		1									
Max7000s	3	3		1									
Spartan2		6	5	1									
Spartan2E		6	5	1									
Spartan3		6	5	1									
Spartan3A		7	6	1									
Spartan3ADSP		7	6	1									
Spartan3AN		7	6	1									
Spartan3E		7	6	1									
Spartan3L		7	6	1									
Virtex		6	5	1									
Virtex2		6	5	1									
Virtex2p		6	5	1									
VirtexE		6	5	1									
Virtex4		7	6	1									
Virtex5		6	1	1									
CoolRunner2	2			1									
CoolRunnerXpla3	2			1									
Xc9500	2			1									
Xc9500XL	2			1									
Xc9500XV	2			1									
ProAsicPlus		18											
ProAsic3		11											
ProAsic3E		11											
Fusion		11											
EC		6		1									
ECP		6	5	1									
ECP2		6	4	1									
ECP2M		6	4	1									
SC		6	4	1									
MACHXO		4	4										
XP		6	5	1									
XP2		6	4	1									

ACC2B

2-Bit Loadable Cascadable Accumulator with Synchronous Reset, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10	2									
Cyclone		21	21	2									1
Cyclone2		10	10	2									
Cyclone3		12	12	2									
Stratix		21	21	2									1
Stratix2		13	13	2									
Stratix3			9	2									1
StratixGX		21	21	2									1
Stratix2GX			10	2									1
Max2		13	13	2									1
Max3000a	12	12		2									
Max7000b	12	12		2									
Max7000ae	12	12		2									
Max7000s	12	12		2									
Spartan2		22	21	2									
Spartan2E		22	21	2									
Spartan3		18	17	2									
Spartan3A		20	19	2									
Spartan3ADSP		18	18	2									
Spartan3AN		20	19	2									
Spartan3E		20	18	2									
Spartan3L		18	17	2									
Virtex		22	21	2									
Virtex2		18	17	2									
Virtex2p		18	17	2									
VirtexE		22	21	2									
Virtex4		18	17	2									
Virtex5		10	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		56											
ProAsic3		32											
ProAsic3E		30											
Fusion		30											
EC		28		2									
ECP		28		2									
ECP2		14	14	2									
ECP2M		14	14	2									
SC		16	14	2									
MACHXO		14	14										
XP		14	14	2									
XP2		14	14	2									

FPGA Arithmetic Function Resource Usage

ACC2S

2-Bit Loadable Cascadable Accumulator with Synchronous Reset, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10	2									
Cyclone		23	23	2								1	
Cyclone2		10	10	2									
Cyclone3		12	12	2									
Stratix		20	20	2								1	
Stratix2		13	13	2									
Stratix3			9	2								1	
StratixGX		20	20	2								1	
Stratix2GX			10	2								1	
Max2		13	13	2								1	
Max3000a	10	10		2									
Max7000b	10	10		2									
Max7000ae	10	10		2									
Max7000s	10	10		2									
Spartan2		22	21	2									
Spartan2E		22	21	2									
Spartan3		18	17	2									
Spartan3A		20	19	2									
Spartan3ADSP		18	18	2									
Spartan3AN		20	19	2									
Spartan3E		20	18	2									
Spartan3L		18	17	2									
Virtex		22	21	2									
Virtex2		18	17	2									
Virtex2p		18	17	2									
VirtexE		22	21	2									
Virtex4		18	17	2									
Virtex5		6	2	2									
CoolRunner2	4			2									
CoolRunnerXpla3	4			2									
Xc9500	4			2									
Xc9500XL	4			2									
Xc9500XV	4			2									
ProAsicPlus		56											
ProAsic3		33											
ProAsic3E		30											
Fusion		30											
EC		22		2									
ECP		22		2									
ECP2		14	14	2									
ECP2M		14	14	2									
SC		16	14	2									
MACHXO		14	14										
XP		14	14	2									
XP2		14	14	2									

**ACC4B**

**4-Bit Loadable Cascadable Accumulator with Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			33	4									
Cyclone		53	53	4								1	
Cyclone2		30	30	4									
Cyclone3		30	30	4									
Stratix		48	48	4								1	
Stratix2		26	26	4									
Stratix3			33	4								1	
StratixGX		48	48	4								1	
Stratix2GX			24	4								1	
Max2		32	32	4								1	
Max3000a	37	37		4									
Max7000b	37	37		4									
Max7000ae	37	37		4									
Max7000s	37	37		4									
Spartan2		44	33	4									
Spartan2E		44	33	4									
Spartan3		34	31	4									
Spartan3A		47	41	5									
Spartan3ADSP		43	38	5									
Spartan3AN		47	41	5									
Spartan3E		36	33	4									
Spartan3L		40	37	4									
Virtex		44	33	4									
Virtex2		34	31	4									
Virtex2p		34	31	4									
VirtexE		44	33	4									
Virtex4		34	30	4									
Virtex5		18	5	5									
CoolRunner2	20			4									
CoolRunnerXpla3	21			4									
Xc9500	32			4									
Xc9500XL	32			4									
Xc9500XV	32			4									
ProAsicPlus		96											
ProAsic3		55											
ProAsic3E		50											
Fusion		49											
EC		56		4									
ECP		56		4									
ECP2		38	33	4									
ECP2M		38	33	4									
SC		36	27	4									
MACHXO		44	43										
XP		34	28	4									
XP2		42	32	4									

**FPGA Arithmetic Function Resource Usage**

**ACC4S**

**4-Bit Loadable Cascadable Accumulator with Synchronous Reset, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			33	4									
Cyclone		51	51	4								1	
Cyclone2		30	30	4									
Cyclone3		30	30	4									
Stratix		51	51	4								1	
Stratix2		26	26	4									
Stratix3			33	4								1	
StratixGX		51	51	4									
Stratix2GX			24	4								1	
Max2		32	32	4								1	
Max3000a	43	43		4									
Max7000b	43	43		4									
Max7000ae	43	43		4									
Max7000s	43	43		4									
Spartan2		44	39	4									
Spartan2E		44	39	4									
Spartan3		34	31	4									
Spartan3A		47	41	5									
Spartan3ADSP		43	38	5									
Spartan3AN		47	41	5									
Spartan3E		36	33	4									
Spartan3L		40	37	4									
Virtex		44	39	4									
Virtex2		34	31	4									
Virtex2p		34	31	4									
VirtexE		44	39	4									
Virtex4		34	30	4									
Virtex5		18	5	5									
CoolRunner2	18			4									
CoolRunnerXpla3	18			4									
Xc9500	23			4									
Xc9500XL	23			4									
Xc9500XV	23			4									
ProAsicPlus		96											
ProAsic3		54											
ProAsic3E		48											
Fusion		49											
EC		56		4									
ECP		56		4									
ECP2		38	33	4									
ECP2M		38	33	4									
SC		36	27	4									
MACHXO		44	43										
XP		34	28	4									
XP2		42	32	4									

**ACC8B**

**8-Bit Loadable Cascadable Accumulator with Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			65	8									
Cyclone		79	79	8									1
Cyclone2		50	50	8									
Cyclone3		52	52	8									
Stratix		78	78	8								1	
Stratix2		46	46	8									
Stratix3			64	8									1
StratixGX		78	78	8									
Stratix2GX			47	8								1	
Max2		53	53	8									1
Max3000a	92	92		8									
Max7000b	92	92		8									
Max7000ae	92	92		8									
Max7000s	92	92		8									
Spartan2		76	57	8									
Spartan2E		76	57	8									
Spartan3		56	52	8									
Spartan3A		81	63	9									
Spartan3ADSP		79	62	9									
Spartan3AN		81	63	9									
Spartan3E		64	61	8									
Spartan3L		76	61	8									
Virtex		76	57	8									
Virtex2		56	52	8									
Virtex2p		56	52	8									
VirtexE		76	57	8									
Virtex4		54	51	8									
Virtex5		36	9	9									
CoolRunner2	36			8									
CoolRunnerXpla3	36			8									
Xc9500	58			8									
Xc9500XL	58			8									
Xc9500XV	58			8									
ProAsicPlus		180											
ProAsic3		120											
ProAsic3E		81											
Fusion		87											
EC		96		8									
ECP		96		8									
ECP2		74	56	8									
ECP2M		74	56	8									
SC		64	47	8									
MACHXO		102	94										
XP		58	48	8									
XP2		70	52	8									

**FPGA Arithmetic Function Resource Usage**

**ACC16B**

**16-Bit Loadable Cascadable Accumulator with Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			129	16									
Cyclone		142	142	16									1
Cyclone2		90	90	16									
Cyclone3		92	92	16									
Stratix		142	142	16									1
Stratix2		86	86	16									
Stratix3			129	16									1
StratixGX		142	142	16									
Stratix2GX			87	16									1
Max2		93	93	16									1
Max3000a	249	249		16									
Max7000b	249	249		16									
Max7000ae	249	249		16									
Max7000s	249	249		16									
Spartan2		140	105	16									
Spartan2E		140	105	16									
Spartan3		104	101	16									
Spartan3A		155	120	17									
Spartan3ADSP		151	118	17									
Spartan3AN		153	119	17									
Spartan3E		120	117	16									
Spartan3L		148	117	16									
Virtex		140	105	16									
Virtex2		104	101	16									
Virtex2p		104	101	16									
VirtexE		140	105	16									
Virtex4		102	99	16									
Virtex5		64	17	17									
CoolRunner2	78			16									
CoolRunnerXpla3	84			16									
Xc9500	118			16									
Xc9500XL	118			16									
Xc9500XV	118			16									
ProAsicPlus		353											
ProAsic3		338											
ProAsic3E		152											
Fusion		166											
EC		176		16									
ECP		176		16									
ECP2		132	96	16									
ECP2M		132	96	16									
SC		120	87	16									
MACHXO		214	182										
XP		122	88	16									
XP2		126	92	16									



**ACC32B**

**32-Bit Loadable Cascadable Accumulator with Synchronous Reset, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			257	32									
Cyclone		270	270	32									1
Cyclone2		171	171	32									
Cyclone3		172	172	32									
Stratix		270	270	32									1
Stratix2		166	166	32									
Stratix3			257	32									1
StratixGX		270	270	32									1
Stratix2GX			167	32									1
Max2		173	173	32									1
Max3000a	425	425		32									
Max7000b	425	425		32									
Max7000ae	425	425		32									
Max7000s	335	335		32									
Spartan2		268	202	32									
Spartan2E		268	202	32									
Spartan3		200	197	32									
Spartan3A		295	230	33									
Spartan3ADSP		293	227	33									
Spartan3AN		295	230	33									
Spartan3E		218	202	32									
Spartan3L		290	226	32									
Virtex		268	202	32									
Virtex2		200	197	32									
Virtex2p		200	197	32									
VirtexE		268	202	32									
Virtex4		198	195	32									
Virtex5		110	35	35									
CoolRunner2	201			32									
CoolRunnerXpla3	995			32									
Xc9500	237			32									
Xc9500XL													
Xc9500XV	240			32									
ProAsicPlus		704											
ProAsic3		572											
ProAsic3E		543											
Fusion		336											
EC		336		32									
ECP		336		32									
ECP2		244	176	32									
ECP2M		244	176	32									
SC		232	167	32									
MACHXO		422	358										
XP		234	168	32									
XP2		238	172	32									

FPGA Arithmetic Function Resource Usage

ADD1

1-Bit Cascadable Full Adder

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		2	2										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		2	2										
Spartan2E		2	2										
Spartan3		2	2										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		2	2										
Virtex2		2	2										
Virtex2p		2	2										
VirtexE		2	2										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		4											
ProAsic3		2											
ProAsic3E		2											
Fusion		2											
EC		2											
ECP		2											
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										

**ADD2B**

**2-Bit Cascadable Full Adder with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		4	4										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5		6											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		14											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		6											
ECP		6											
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

FPGA Arithmetic Function Resource Usage

**ADD2S**

**2-Bit Cascadable Full Adder with Signed and Unsigned Operations, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		5	5										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		5	5										
Stratix2		4	4										
Stratix3			4										
StratixGX		5	5										
Stratix2GX			4										
Max2		5	5										
Max3000a	8	8											
Max7000b	8	8											
Max7000ae	8	8											
Max7000s	8	8											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		6	5										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		6	5										
Virtex2p		6	5										
VirtexE		6	5										
Virtex4		6	5										
Virtex5		4											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		14											
ProAsic3		5											
ProAsic3E		5											
Fusion		5											
EC		6											
ECP		6											
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

**ADD4B**

**4-Bit Cascadable Full Adder with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7										
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3			7										
StratixGX		7	7										
Stratix2GX			7										
Max2		7	7										
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		12	9										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		12	9										
Virtex2p		12	9										
VirtexE		6	5										
Virtex4		12	9										
Virtex5			4										
CoolRunner2	7												
CoolRunnerXpla3	7												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		26											
ProAsic3		9											
ProAsic3E		9											
Fusion		9											
EC		6											
ECP		6											
ECP2		12	9										
ECP2M		12	9										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		10	8										

**FPGA Arithmetic Function Resource Usage**

**ADD4S**

**4-Bit Cascadable Full Adder with Signed and Unsigned Operations, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7										
Cyclone		7	7										
Cyclone2		7	7										
Cyclone3		7	7										
Stratix		7	7										
Stratix2		7	7										
Stratix3			7										
StratixGX		7	7										
Stratix2GX			7										
Max2		7	7										
Max3000a	12	12											
Max7000b	12	12											
Max7000ae	12	12											
Max7000s	12	12											
Spartan2		6	5										
Spartan2E		6	5										
Spartan3		12	9										
Spartan3A		6	5										
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5										
Spartan3L		6	5										
Virtex		6	5										
Virtex2		12	9										
Virtex2p		12	9										
VirtexE		6	5										
Virtex4		12	9										
Virtex5		4											
CoolRunner2	7												
CoolRunnerXpla3	7												
Xc9500	8												
Xc9500XL	8												
Xc9500XV	8												
ProAsicPlus		26											
ProAsic3	9												
ProAsic3E	9												
Fusion	9												
EC	6												
ECP	6												
ECP2	12	9											
ECP2M	12	9											
SC	6	5											
MACHXO	6	5											
XP	6	5											
XP2	10	8											

**ADD8B**

**8-Bit Cascadable Full Adder with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			11										
Cyclone		11	11										
Cyclone2		11	11										
Cyclone3		11	11										
Stratix		11	11										
Stratix2		11	11										
Stratix3			11										
StratixGX		11	11										
Stratix2GX			11										
Max2		11	11										
Max3000a	24	24											
Max7000b	24	24											
Max7000ae	24	24											
Max7000s	24	24											
Spartan2		10	9										
Spartan2E		10	9										
Spartan3		10	9										
Spartan3A		10	9										
Spartan3ADSP		10	9										
Spartan3AN		10	9										
Spartan3E		10	9										
Spartan3L		10	9										
Virtex		10	9										
Virtex2		10	9										
Virtex2p		10	9										
VirtexE		10	9										
Virtex4		10	9										
Virtex5			6										
CoolRunner2	19												
CoolRunnerXpla3	19												
Xc9500	14												
Xc9500XL	14												
Xc9500XV	14												
ProAsicPlus		52											
ProAsic3		17											
ProAsic3E		17											
Fusion		17											
EC		10											
ECP		10											
ECP2		16	13										
ECP2M		16	13										
SC		10	9										
MACHXO		10	9										
XP		10	9										
XP2		14	12										

**FPGA Arithmetic Function Resource Usage**

**ADD16B**

**16-Bit Cascadable Full Adder with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			19										
Cyclone		19	19										
Cyclone2		19	19										
Cyclone3		19	19										
Stratix		19	19										
Stratix2		19	19										
Stratix3			19										
StratixGX		19	19										
Stratix2GX			19										
Max2		19	19										
Max3000a	55	55											
Max7000b	55	55											
Max7000ae	55	55											
Max7000s	55	55											
Spartan2		18	17										
Spartan2E		18	17										
Spartan3		18	17										
Spartan3A		18	17										
Spartan3ADSP		18	17										
Spartan3AN		18	17										
Spartan3E		18	17										
Spartan3L		18	17										
Virtex		18	17										
Virtex2		18	17										
Virtex2p		18	17										
VirtexE		18	17										
Virtex4		18	17										
Virtex5		10											
CoolRunner2	45												
CoolRunnerXpla3	45												
Xc9500	32												
Xc9500XL	32												
Xc9500XV	32												
ProAsicPlus		106											
ProAsic3		33											
ProAsic3E		33											
Fusion		33											
EC		18											
ECP		18											
ECP2		24	21										
ECP2M		24	21										
SC		18	17										
MACHXO		18	17										
XP		18	17										
XP2		22	20										



**ADD32B**

**32-Bit Cascadable Full Adder with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			35										
Cyclone		35	35										
Cyclone2		35	35										
Cyclone3		35	35										
Stratix		35	35										
Stratix2		35	35										
Stratix3			35										
StratixGX		35	35										
Stratix2GX			35										
Max2		35	35										
Max3000a	128	128											
Max7000b	128	128											
Max7000ae	128	128											
Max7000s	128	128											
Spartan2		34	33										
Spartan2E		34	33										
Spartan3		34	33										
Spartan3A		34	33										
Spartan3ADSP		34	33										
Spartan3AN		34	33										
Spartan3E		34	33										
Spartan3L		34	33										
Virtex		34	33										
Virtex2		34	33										
Virtex2p		34	33										
VirtexE		34	33										
Virtex4		34	33										
Virtex5		18											
CoolRunner2	111												
CoolRunnerXpla3	105												
Xc9500	69												
Xc9500XL	69												
Xc9500XV	69												
ProAsicPlus		216											
ProAsic3		67											
ProAsic3E		65											
Fusion		65											
EC		34											
ECP		34											
ECP2		40	37										
ECP2M		40	37										
SC		34	33										
MACHXO		34	33										
XP		34	33										
XP2		38	36										

**FPGA Arithmetic Function Resource Usage**

**ADDF2B**

**2-Bit Cascadable Unsigned Binary Full Adder, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		3	3										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	4										
Spartan2E		6	4										
Spartan3		6	4										
Spartan3A		6	4										
Spartan3ADSP		6	4										
Spartan3AN		6	4										
Spartan3E		6	4										
Spartan3L		6	4										
Virtex		6	4										
Virtex2		6	4										
Virtex2p		6	4										
VirtexE		6	4										
Virtex4		6	4										
Virtex5			4										
CoolRunner2	3												
CoolRunnerXpla3	3												
Xc9500	3												
Xc9500XL	3												
Xc9500XV	3												
ProAsicPlus		11											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4											
ECP		4											
ECP2		4	4										
ECP2M		4	4										
SC		6	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

## ADDF2S

### 2-Bit Cascadable Unsigned Binary Full Adder, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		3	3										
Stratix3			3										
StratixGX		4	4										
Stratix2GX			3										
Max2		4	4										
Max3000a	6	6											
Max7000b	6	6											
Max7000ae	6	6											
Max7000s	6	6											
Spartan2		6	4										
Spartan2E		6	4										
Spartan3		6	4										
Spartan3A		6	4										
Spartan3ADSP		6	4										
Spartan3AN		6	4										
Spartan3E		6	4										
Spartan3L		6	4										
Virtex		6	4										
Virtex2		6	4										
Virtex2p		6	4										
VirtexE		6	4										
Virtex4		6	4										
Virtex5			4										
CoolRunner2	3												
CoolRunnerXpla3	3												
Xc9500	3												
Xc9500XL	3												
Xc9500XV	3												
ProAsicPlus		11											
ProAsic3		4											
ProAsic3E		4											
Fusion		4											
EC		4											
ECP		4											
ECP2		4	4										
ECP2M		4	4										
SC		6	4										
MACHXO		4	4										
XP		4	4										
XP2		4	4										

FPGA Arithmetic Function Resource Usage

**ADDF4B**

**4-Bit Cascadable Unsigned Binary Full Adder, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6										
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3			6										
StratixGX		6	6										
Stratix2GX			6										
Max2		6	6										
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		12	8										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		12	8										
Virtex2p		12	8										
VirtexE		4	4										
Virtex4		12	8										
Virtex5		2											
CoolRunner2	6												
CoolRunnerXpla3	6												
Xc9500	7												
Xc9500XL	7												
Xc9500XV	7												
ProAsicPlus		23											
ProAsic3	8												
ProAsic3E	8												
Fusion	8												
EC	4												
ECP	4												
ECP2	10	8											
ECP2M	10	8											
SC	4	4											
MACHXO	4	4											
XP	4	4											
XP2	8	7											

## ADDF4S

### 4-Bit Cascadable Unsigned Binary Full Adder, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6										
Cyclone		6	6										
Cyclone2		6	6										
Cyclone3		6	6										
Stratix		6	6										
Stratix2		6	6										
Stratix3			6										
StratixGX		6	6										
Stratix2GX			6										
Max2		6	6										
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		4	4										
Spartan2E		4	4										
Spartan3		12	8										
Spartan3A		4	4										
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4										
Spartan3L		4	4										
Virtex		4	4										
Virtex2		12	8										
Virtex2p		12	8										
VirtexE		4	4										
Virtex4		12	8										
Virtex5		2											
CoolRunner2	6												
CoolRunnerXpla3	6												
Xc9500	7												
Xc9500XL	7												
Xc9500XV	7												
ProAsicPlus		23											
ProAsic3	8												
ProAsic3E	8												
Fusion	8												
EC	4												
ECP	4												
ECP2	10	8											
ECP2M	10	8											
SC	4	4											
MACHXO	4	4											
XP	4	4											
XP2	8	7											

FPGA Arithmetic Function Resource Usage

**ADDF8B**

**8-Bit Cascadable Unsigned Binary Full Adder, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10										
Cyclone		10	10										
Cyclone2		10	10										
Cyclone3		10	10										
Stratix		10	10										
Stratix2		10	10										
Stratix3			10										
StratixGX		10	10										
Stratix2GX			10										
Max2		10	10										
Max3000a	23	23											
Max7000b	23	23											
Max7000ae	23	23											
Max7000s	23	23											
Spartan2		8	8										
Spartan2E		8	8										
Spartan3		8	8										
Spartan3A		8	8										
Spartan3ADSP		8	8										
Spartan3AN		8	8										
Spartan3E		8	8										
Spartan3L		8	8										
Virtex		8	8										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		8	8										
Virtex4		8	8										
Virtex5			4										
CoolRunner2	18												
CoolRunnerXpla3	18												
Xc9500	12												
Xc9500XL	12												
Xc9500XV	12												
ProAsicPlus		49											
ProAsic3		16											
ProAsic3E		16											
Fusion		16											
EC		8											
ECP		8											
ECP2		14	12										
ECP2M		14	12										
SC		8	8										
MACHXO		8	8										
XP		8	8										
XP2		12	11										

**ADDF16B**

**16-Bit Cascadable Unsigned Binary Full Adder, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			18										
Cyclone		18	18										
Cyclone2		18	18										
Cyclone3		18	18										
Stratix		18	18										
Stratix2		18	18										
Stratix3			18										
StratixGX		18	18										
Stratix2GX			18										
Max2		18	18										
Max3000a	52	52											
Max7000b	52	52											
Max7000ae	52	52											
Max7000s	52	52											
Spartan2		16	16										
Spartan2E		16	16										
Spartan3		16	16										
Spartan3A		16	16										
Spartan3ADSP		16	16										
Spartan3AN		16	16										
Spartan3E		16	16										
Spartan3L		16	16										
Virtex		16	16										
Virtex2		16	16										
Virtex2p		16	16										
VirtexE		16	16										
Virtex4		16	16										
Virtex5		8											
CoolRunner2	50												
CoolRunnerXpla3	50												
Xc9500	30												
Xc9500XL	30												
Xc9500XV	30												
ProAsicPlus		103											
ProAsic3		32											
ProAsic3E		32											
Fusion		32											
EC		16											
ECP		16											
ECP2		22	20										
ECP2M		22	20										
SC		16	16										
MACHXO		16	16										
XP		16	16										
XP2		20	19										

**FPGA Arithmetic Function Resource Usage**

**ADDF32B**

**32-Bit Cascadable Unsigned Binary Full Adder, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			34										
Cyclone		34	34										
Cyclone2		34	34										
Cyclone3		34	34										
Stratix		34	34										
Stratix2		34	34										
Stratix3			34										
StratixGX		34	34										
Stratix2GX			34										
Max2		34	34										
Max3000a	124	124											
Max7000b	124	124											
Max7000ae	124	124											
Max7000s	124	124											
Spartan2		32	32										
Spartan2E		32	32										
Spartan3		32	32										
Spartan3A		32	32										
Spartan3ADSP		32	32										
Spartan3AN		32	32										
Spartan3E		32	32										
Spartan3L		32	32										
Virtex		32	32										
Virtex2		32	32										
Virtex2p		32	32										
VirtexE		32	32										
Virtex4		32	32										
Virtex5		16											
CoolRunner2	86												
CoolRunnerXpla3	86												
Xc9500	67												
Xc9500XL	67												
Xc9500XV	67												
ProAsicPlus		213											
ProAsic3		66											
ProAsic3E		64											
Fusion		64											
EC		32											
ECP		32											
ECP2		38	36										
ECP2M		38	36										
SC		32	32										
MACHXO		32	32										
XP		32	32										
XP2		36	35										



**ADDFR2B**

**2-Bit Cascadable Unsigned Binary Registered Full Adder, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	3									
Cyclone		4	4	3									1
Cyclone2		4	4	3									
Cyclone3		4	4	3									
Stratix		4	4	3									1
Stratix2		3	3	3									
Stratix3			3	3									1
StratixGX		4	4	3									1
Stratix2GX			3	3									1
Max2		4	4	3									1
Max3000a	6	6		3									
Max7000b	6	6		3									
Max7000ae	6	6		3									
Max7000s	6	6		3									
Spartan2		9	7	3									
Spartan2E		9	7	3									
Spartan3		9	7	3									
Spartan3A		9	7	3									
Spartan3ADSP		9	7										
Spartan3AN		9	7										
Spartan3E		9	7	3									
Spartan3L		9	7	3									
Virtex		9	7	3									
Virtex2		9	7	3									
Virtex2p		9	7	3									
VirtexE		9	7	3									
Virtex4		9	7	3									
Virtex5		7	3	3									
CoolRunner2	3			3									
CoolRunnerXpla3	3			3									
Xc9500	3			3									
Xc9500XL	3			3									
Xc9500XV	3			3									
ProAsicPlus		14											
ProAsic3		7											
ProAsic3E		7											
Fusion		4											
EC		6		3									
ECP		6		3									
ECP2		6	4	3									
ECP2M		6	4	3									
SC		6	4	3									
MACHXO		6	4										
XP		6	4	3									
XP2		6	4	3									

**FPGA Arithmetic Function Resource Usage**

**ADDFR2S**

**2-Bit Cascadable Unsigned Binary Registered Full Adder, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			3	3									
Cyclone		4	4	3									1
Cyclone2		4	4	3									
Cyclone3		4	4	3									
Stratix		4	4	3									1
Stratix2		3	3	3									
Stratix3			3	3									1
StratixGX		4	4	3									1
Stratix2GX			3	3									1
Max2		4	4	3									1
Max3000a	6	6		3									
Max7000b	6	6		3									
Max7000ae	6	6		3									
Max7000s	6	6		3									
Spartan2		9	7	3									
Spartan2E		9	7	3									
Spartan3		9	7	3									
Spartan3A		9	7	3									
Spartan3ADSP		9	7										
Spartan3AN		9	7										
Spartan3E		9	7	3									
Spartan3L		9	7	3									
Virtex		9	7	3									
Virtex2		9	7	3									
Virtex2p		9	7	3									
VirtexE		9	7	3									
Virtex4		9	7	3									
Virtex5		7	3	3									
CoolRunner2	3			3									
CoolRunnerXpla3	3			3									
Xc9500	3			3									
Xc9500XL	3			3									
Xc9500XV	3			3									
ProAsicPlus		14											
ProAsic3		7											
ProAsic3E		7											
Fusion		4											
EC		6		3									
ECP		6		3									
ECP2		6	4	3									
ECP2M		6	4	3									
SC		6	4	3									
MACHXO		6	4										
XP		6	4	3									
XP2		6	4	3									

## ADDFR4B

### 4-Bit Cascadable Unsigned Binary Registered Full Adder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	5									
Cyclone		6	6	5								1	
Cyclone2		6	6	5									
Cyclone3		6	6	5									
Stratix		6	6	5								1	
Stratix2		6	6	5									
Stratix3			6	5								1	
StratixGX		6	6	5								1	
Stratix2GX			6	5								1	
Max2		7	6	5								1	
Max3000a	10	10		5									
Max7000b	10	10		5									
Max7000ae	10	10		5									
Max7000s	10	10		5									
Spartan2		11	9	5									
Spartan2E		11	9	5									
Spartan3		17	14	5									
Spartan3A		7	5	1									
Spartan3ADSP		7	6	1									
Spartan3AN		7	6	1									
Spartan3E		7	5	1									
Spartan3L		7	5	1									
Virtex		11	9	5									
Virtex2		17	14	5									
Virtex2p		17	14	5									
VirtexE		11	9	5									
Virtex4		19	14	5									
Virtex5		8	4	1									
CoolRunner2	6			5									
CoolRunnerXpla3	6			5									
Xc9500	7			5									
Xc9500XL	7			5									
Xc9500XV	7			5									
ProAsicPlus		28											
ProAsic3		13											
ProAsic3E		13											
Fusion		8											
EC		6		5									
ECP		6		5									
ECP2		10	8	5									
ECP2M		10	8	5									
SC		6	4	5									
MACHXO		6	4										
XP		6	4	5									
XP2		8	7	5									

**FPGA Arithmetic Function Resource Usage**

**ADDFR4S**

**4-Bit Cascadable Unsigned Binary Registered Full Adder, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			6	5									
Cyclone		6	6	5									1
Cyclone2		6	6	5									
Cyclone3		6	6	5									
Stratix		6	6	5									1
Stratix2		6	6	5									
Stratix3			6	5									1
StratixGX		6	6	5									1
Stratix2GX			6	5									1
Max2		7	6	5									1
Max3000a	10	10		5									
Max7000b	10	10		5									
Max7000ae	10	10		5									
Max7000s	10	10		5									
Spartan2		11	9	5									
Spartan2E		11	9	5									
Spartan3		17	14	5									
Spartan3A		7	5	1									
Spartan3ADSP		7	6	1									
Spartan3AN		7	6	1									
Spartan3E		7	5	1									
Spartan3L		7	5	1									
Virtex		11	9	5									
Virtex2		17	14	5									
Virtex2p		17	14	5									
VirtexE		11	9	5									
Virtex4		19	14	5									
Virtex5		8	4	1									
CoolRunner2	6			5									
CoolRunnerXpla3	6			5									
Xc9500	7			5									
Xc9500XL	7			5									
Xc9500XV	7			5									
ProAsicPlus		28											
ProAsic3		13											
ProAsic3E		13											
Fusion		8											
EC		6		5									
ECP		6		5									
ECP2		10	8	5									
ECP2M		10	8	5									
SC		6	4	5									
MACHXO		6	4										
XP		6	4	5									
XP2		8	7	5									

## ADDFR8B

### 8-Bit Cascadable Unsigned Binary Registered Full Adder, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			10	9									
Cyclone		10	10	9									1
Cyclone2		10	10	9									
Cyclone3		10	10	9									
Stratix		10	10	9									1
Stratix2		10	10	9									
Stratix3			10	9									1
StratixGX		10	10	9									1
Stratix2GX			10	9									1
Max2		11	10	9									1
Max3000a	23	23		9									
Max7000b	23	23		9									
Max7000ae	23	23		9									
Max7000s	23	23		9									
Spartan2		19	17	9									
Spartan2E		19	17	9									
Spartan3		19	17	9									
Spartan3A		11	9	1									
Spartan3ADSP		11	10	1									
Spartan3AN		11	10	1									
Spartan3E		11	9	1									
Spartan3L		11	9	1									
Virtex		19	17	9									
Virtex2		19	17	9									
Virtex2p		19	17	9									
VirtexE		19	17	9									
Virtex4		19	17	9									
Virtex5		14	8	1									
CoolRunner2	18			9									
CoolRunnerXpla3	18			9									
Xc9500	12			9									
Xc9500XL	12			9									
Xc9500XV	12			9									
ProAsicPlus		58											
ProAsic3		25											
ProAsic3E		25											
Fusion		16											
EC		10		9									
ECP		10		9									
ECP2		14	12	9									
ECP2M		14	12	9									
SC		10	8	9									
MACHXO		10	8										
XP		10	8	9									
XP2		12	11	9									

**FPGA Arithmetic Function Resource Usage**

**ADDFR16B**

**16-Bit Cascadable Unsigned Binary Registered Full Adder, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			18	17									
Cyclone		18	18	17									1
Cyclone2		18	18	17									
Cyclone3		18	18	17									
Stratix		18	18	17								1	
Stratix2		18	18	17									
Stratix3			18	17									1
StratixGX		18	18	17									1
Stratix2GX			18	17									1
Max2		19	18	17									1
Max3000a	52	52		17									
Max7000b	52	52		17									
Max7000ae	52	52		17									
Max7000s	52	52		17									
Spartan2		35	33	17									
Spartan2E		35	33	17									
Spartan3		35	33	17									
Spartan3A		19	17	1									
Spartan3ADSP		19	18	1									
Spartan3AN		19	18	1									
Spartan3E		19	17	1									
Spartan3L		19	17	1									
Virtex		35	33	17									
Virtex2		35	33	17									
Virtex2p		35	33	17									
VirtexE		35	33	17									
Virtex4		35	33	17									
Virtex5		26	16	1									
CoolRunner2	50			17									
CoolRunnerXpla3	50			17									
Xc9500	30			17									
Xc9500XL	30			17									
Xc9500XV	30			17									
ProAsicPlus		120											
ProAsic3		50											
ProAsic3E		50											
Fusion		32											
EC		18		17									
ECP		18		17									
ECP2		22	20	17									
ECP2M		22	20	17									
SC		18	16	17									
MACHXO		18	16										
XP		18	16	17									
XP2		20	19	17									

**ADDFR32B**

**32-Bit Cascadable Unsigned Binary Registered Full Adder, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			34	33									
Cyclone		34	34	33									1
Cyclone2		34	34	33									
Cyclone3		34	34	33									
Stratix		34	34	33									1
Stratix2		34	34	33									
Stratix3			34	33									1
StratixGX		34	34	33									1
Stratix2GX			34	33									1
Max2		35	34	33									1
Max3000a	124	124		33									
Max7000b	124	124		33									
Max7000ae	124	124		33									
Max7000s	124	124		33									
Spartan2		67	65	33									
Spartan2E		67	65	33									
Spartan3		67	65	33									
Spartan3A		35	33	1									
Spartan3ADSP		35	34	1									
Spartan3AN		35	34	1									
Spartan3E		35	33	1									
Spartan3L		35	33	1									
Virtex		67	65	33									
Virtex2		67	65	33									
Virtex2p		67	65	33									
VirtexE		67	65	33									
Virtex4		67	65	33									
Virtex5		50	32	1									
CoolRunner2	86			33									
CoolRunnerXpla3	86			33									
Xc9500	67			33									
Xc9500XL	67			33									
Xc9500XV	67			33									
ProAsicPlus		246											
ProAsic3		101											
ProAsic3E		100											
Fusion		64											
EC		34		33									
ECP		34		33									
ECP2		38	36	33									
ECP2M		38	36	33									
SC		34	32	33									
MACHXO		34	32										
XP		34	32	33									
XP2		36	35	33									

**FPGA Arithmetic Function Resource Usage**

**ADDR1**

**1-Bit Cascadable Registered Full Adder**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2									1
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2									1
Stratix2		2	2	2									
Stratix3			2	2									1
StratixGX		2	2	2									
Stratix2GX			2	2									1
Max2		2	2	2									1
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		4	4	2									
Spartan2E		4	4	2									
Spartan3		4	4	2									
Spartan3A		4	4	2									
Spartan3ADSP		4	4										
Spartan3AN		4	4										
Spartan3E		4	4	2									
Spartan3L		4	4	2									
Virtex		4	4	2									
Virtex2		4	4	2									
Virtex2p		4	4	2									
VirtexE		4	4	2									
Virtex4		4	4	2									
Virtex5		4	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		6											
ProAsic3		4											
ProAsic3E		4											
Fusion		2											
EC		4		2									
ECP		4		2									
ECP2		4	2	2									
ECP2M		4	2	2									
SC		4	2	2									
MACHXO		4	2										
XP		4	2	2									
XP2		4	2	2									



## ADDR2B

### 2-Bit Cascadable Registered Full Adder with Signed and Unsigned Operations, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		5	5	4								1	
Cyclone2		5	5	4									
Cyclone3		5	5	4									
Stratix		5	5	4								1	
Stratix2		4	4	4									
Stratix3			4	4								1	
StratixGX		5	5	4								1	
Stratix2GX			4	4								1	
Max2		5	5	4								1	
Max3000a	8	8		4									
Max7000b	8	8		4									
Max7000ae	8	8		4									
Max7000s	8	8		4									
Spartan2		10	10	4									
Spartan2E		10	10	4									
Spartan3		10	10	4									
Spartan3A		10	9	4									
Spartan3ADSP		10	9										
Spartan3AN		10	9										
Spartan3E		10	9	4									
Spartan3L		10	9	4									
Virtex		10	10	4									
Virtex2		10	10	4									
Virtex2p		10	10	4									
VirtexE		10	10	4									
Virtex4		12	10	4									
Virtex5		8	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		18											
ProAsic3		9											
ProAsic3E		9											
Fusion		5											
EC		8		4									
ECP		8		4									
ECP2		8	5	4									
ECP2M		8	5	4									
SC		8	5	4									
MACHXO		8	5										
XP		8	5	4									
XP2		8	5	4									

FPGA Arithmetic Function Resource Usage

**ADDR2S**

**2-Bit Cascadable Registered Full Adder with Signed and Unsigned Operations, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		5	5	4								1	
Cyclone2		5	5	4									
Cyclone3		5	5	4									
Stratix		5	5	4								1	
Stratix2		4	4	4									
Stratix3			4	4								1	
StratixGX		5	5	4									
Stratix2GX			4	4								1	
Max2		5	5	4								1	
Max3000a	8	8		4									
Max7000b	8	8		4									
Max7000ae	8	8		4									
Max7000s	8	8		4									
Spartan2		10	10	4									
Spartan2E		10	10	4									
Spartan3		10	10	4									
Spartan3A		10	9	4									
Spartan3ADSP		10	9										
Spartan3AN		10	9										
Spartan3E		10	9	4									
Spartan3L		10	9	4									
Virtex		10	10	4									
Virtex2		10	10	4									
Virtex2p		10	10	4									
VirtexE		10	10	4									
Virtex4		12	10	4									
Virtex5		10	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		18											
ProAsic3		9											
ProAsic3E		9											
Fusion		5											
EC		8		4									
ECP		8		4									
ECP2		8	5	4									
ECP2M		8	5	4									
SC		8	5	4									
MACHXO		8	5										
XP		8	5	4									
XP2		8	5	4									

## ADDR4B

### 4-Bit Cascadable Registered Full Adder with Signed and Unsigned Operations, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	6									
Cyclone		7	7	6									1
Cyclone2		7	7	6									
Cyclone3		7	7	6									
Stratix		7	7	6									1
Stratix2		7	7	6									
Stratix3			7	6									1
StratixGX		9	7	6									
Stratix2GX			7	6									1
Max2		9	7	6									1
Max3000a	12	12		6									
Max7000b	12	12		6									
Max7000ae	12	12		6									
Max7000s	12	12		6									
Spartan2		14	12	6									
Spartan2E		14	12	6									
Spartan3		20	17	6									
Spartan3A		9	6	1									
Spartan3ADSP		9	7	1									
Spartan3AN		9	7	1									
Spartan3E		9	6	1									
Spartan3L		9	6	1									
Virtex		14	12	6									
Virtex2		20	17	6									
Virtex2p		20	17	6									
VirtexE		14	12	6									
Virtex4		22	17	6									
Virtex5		11	5	1									
CoolRunner2	7			6									
CoolRunnerXpla3	7			6									
Xc9500	8			6									
Xc9500XL	8			6									
Xc9500XV	8			6									
ProAsicPlus		32											
ProAsic3		15											
ProAsic3E		15											
Fusion		9											
EC		12		6									
ECP		12		6									
ECP2		12	9	6									
ECP2M		12	9	6									
SC		8	5	6									
MACHXO		12	5										
XP		12	5	6									
XP2		10	8	6									

**FPGA Arithmetic Function Resource Usage**

**ADDR4S**

**4-Bit Cascadable Registered Full Adder with Signed and Unsigned Operations,  
Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7	6									
Cyclone		7	7	6									1
Cyclone2		7	7	6									
Cyclone3		7	7	6									
Stratix		7	7	6									1
Stratix2		7	7	6									
Stratix3			7	6									1
StratixGX		7	7	6									1
Stratix2GX			7	6									1
Max2		9	7	6									1
Max3000a	12	12		6									
Max7000b	12	12		6									
Max7000ae	12	12		6									
Max7000s	12	12		6									
Spartan2		14	12	6									
Spartan2E		14	12	6									
Spartan3		20	17	6									
Spartan3A		9	6	1									
Spartan3ADSP		9	7	1									
Spartan3AN		9	7	1									
Spartan3E		9	6	1									
Spartan3L		9	6	1									
Virtex		14	12	6									
Virtex2		20	17	6									
Virtex2p		20	17	6									
VirtexE		14	12	6									
Virtex4		22	17	6									
Virtex5		11	5	1									
CoolRunner2	7			6									
CoolRunnerXpla3	7			6									
Xc9500	8			6									
Xc9500XL	8			6									
Xc9500XV	8			6									
ProAsicPlus		32											
ProAsic3		15											
ProAsic3E		15											
Fusion		9											
EC		12		6									
ECP		12		6									
ECP2		12	9	6									
ECP2M		12	9	6									
SC		8	5	6									
MACHXO		12	5										
XP		12	5	6									
XP2		10	8	6									

## ADDR8B

### 8-Bit Cascadable Registered Full Adder with Signed and Unsigned Operations, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			11	10									
Cyclone		11	11	10									1
Cyclone2		11	11	10									
Cyclone3		11	11	10									
Stratix		11	11	10									1
Stratix2		11	11	10									
Stratix3			11	10									1
StratixGX		11	11	10									1
Stratix2GX			11	10									1
Max2		13	11	10									1
Max3000a	24	24		10									
Max7000b	24	24		10									
Max7000ae	24	24		10									
Max7000s	24	24		10									
Spartan2		22	20	10									
Spartan2E		22	20	10									
Spartan3		22	20	10									
Spartan3A		13	10	1									
Spartan3ADSP		13	11	1									
Spartan3AN		13	11	1									
Spartan3E		13	10	1									
Spartan3L		13	10	1									
Virtex		22	20	10									
Virtex2		22	20	10									
Virtex2p		22	20	10									
VirtexE		22	20	10									
Virtex4		22	20	10									
Virtex5		17	9	1									
CoolRunner2	19			10									
CoolRunnerXpla3	19			10									
Xc9500	14			10									
Xc9500XL	14			10									
Xc9500XV	14			10									
ProAsicPlus		62											
ProAsic3		27											
ProAsic3E		27											
Fusion		17											
EC		16		10									
ECP		16		10									
ECP2		16	13	10									
ECP2M		16	13	10									
SC		12	9	10									
MACHXO		16	9										
XP		16	9	10									
XP2		14	12	10									

**FPGA Arithmetic Function Resource Usage**

**ADDR16B**

**16-Bit Cascadable Registered Full Adder with Signed and Unsigned Operations,  
Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			19	18									
Cyclone		19	19	18									1
Cyclone2		19	19	18									
Cyclone3		19	19	18									
Stratix		19	19	18									1
Stratix2		19	19	18									
Stratix3			19	18									1
StratixGX		19	19	18									1
Stratix2GX			19	18									1
Max2		21	19	18									1
Max3000a	55	55		18									
Max7000b	55	55		18									
Max7000ae	55	55		18									
Max7000s	55	55		18									
Spartan2		38	36	18									
Spartan2E		38	36	18									
Spartan3		38	36	18									
Spartan3A		21	18	1									
Spartan3ADSP		21	19	1									
Spartan3AN		21	19	1									
Spartan3E		21	18	1									
Spartan3L		21	18	1									
Virtex		38	36	18									
Virtex2		38	36	18									
Virtex2p		38	36	18									
VirtexE		38	36	18									
Virtex4		38	36	18									
Virtex5		29	17	1									
CoolRunner2	39			18									
CoolRunnerXpla3	39			18									
Xc9500	32			18									
Xc9500XL	32			18									
Xc9500XV	32			18									
ProAsicPlus		124											
ProAsic3		52											
ProAsic3E		52											
Fusion		33											
EC		24		18									
ECP		24		18									
ECP2		24	21	18									
ECP2M		24	21	18									
SC		20	17	18									
MACHXO		24	17										
XP		24	17	18									
XP2		22	20	18									

## ADDR32B

### 32-Bit Cascadable Registered Full Adder with Signed and Unsigned Operations, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			35	34									
Cyclone		35	35	34								1	
Cyclone2		35	35	34									
Cyclone3		35	35	34									
Stratix		35	35	34								1	
Stratix2		35	35	34									
Stratix3			35	34								1	
StratixGX		35	35	34								1	
Stratix2GX			35	34								1	
Max2		37	35	34								1	
Max3000a	128	128		34									
Max7000b	128	128		34									
Max7000ae	128	128		34									
Max7000s	128	128		34									
Spartan2		70	68	34									
Spartan2E		70	68	34									
Spartan3		70	68	34									
Spartan3A		37	34	1									
Spartan3ADSP		37	35	1									
Spartan3AN		37	35	1									
Spartan3E		37	34	1									
Spartan3L		37	34	1									
Virtex		70	68	34									
Virtex2		70	68	34									
Virtex2p		70	68	34									
VirtexE		70	68	34									
Virtex4		70	68	34									
Virtex5		53	33	1									
CoolRunner2	109			34									
CoolRunnerXpla3	202			34									
Xc9500	69			34									
Xc9500XL	69			34									
Xc9500XV	69			34									
ProAsicPlus		250											
ProAsic3		103											
ProAsic3E		101											
Fusion		65											
EC		40		34									
ECP		40		34									
ECP2		40	37	34									
ECP2M		40	37	34									
SC		36	33	34									
MACHXO		40	33										
XP		40	33	34									
XP2		38	36	34									

**FPGA Arithmetic Function Resource Usage**

**ADSU1**

**1-Bit Cascadable Full Adder/Subtractor**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2										
Cyclone		2	2										
Cyclone2		2	2										
Cyclone3		2	2										
Stratix		2	2										
Stratix2		4	4										
Stratix3			2										
StratixGX		2	2										
Stratix2GX			2										
Max2		2	2										
Max3000a	2	2											
Max7000b	2	2											
Max7000ae	2	2											
Max7000s	2	2											
Spartan2		4	3										
Spartan2E		4	3										
Spartan3		4	3										
Spartan3A		2	2										
Spartan3ADSP		2	2										
Spartan3AN		2	2										
Spartan3E		2	2										
Spartan3L		2	2										
Virtex		4	3										
Virtex2		4	3										
Virtex2p		4	3										
VirtexE		4	3										
Virtex4		2	2										
Virtex5		2											
CoolRunner2	2												
CoolRunnerXpla3	2												
Xc9500	2												
Xc9500XL	2												
Xc9500XV	2												
ProAsicPlus		15											
ProAsic3		5											
ProAsic3E		3											
Fusion		3											
EC		2											
ECP		2											
ECP2		2	2										
ECP2M		2	2										
SC		2	2										
MACHXO		2	2										
XP		2	2										
XP2		2	2										



**ADSU2B**

**2-Bit Cascadable Full Adder/Subtractor with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7										
Cyclone		6	6										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		6	6										
Stratix2		7	7										
Stratix3			7										
StratixGX		6	6										
Stratix2GX			5										
Max2		5	5										
Max3000a	11	11											
Max7000b	11	11											
Max7000ae	11	11											
Max7000s	11	11											
Spartan2		10	10										
Spartan2E		10	10										
Spartan3		8	8										
Spartan3A		10	10										
Spartan3ADSP		10	10										
Spartan3AN		10	10										
Spartan3E		6	5										
Spartan3L		10	10										
Virtex		10	10										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		10	10										
Virtex4		6	5										
Virtex5		8											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		33											
ProAsic3		10											
ProAsic3E		7											
Fusion		7											
EC		20											
ECP		20											
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

FPGA Arithmetic Function Resource Usage

ADSU2S

2-Bit Cascadable Full Adder/Subtractor with Signed and Unsigned Operations,  
Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			7										
Cyclone		6	6										
Cyclone2		5	5										
Cyclone3		5	5										
Stratix		6	6										
Stratix2		7	7										
Stratix3			7										
StratixGX		6	6										
Stratix2GX			5										
Max2		5	5										
Max3000a	10	10											
Max7000b	10	10											
Max7000ae	10	10											
Max7000s	10	10											
Spartan2		12	12										
Spartan2E		12	12										
Spartan3		8	8										
Spartan3A		10	10										
Spartan3ADSP		10	10										
Spartan3AN		10	10										
Spartan3E		6	5										
Spartan3L		10	10										
Virtex		12	12										
Virtex2		8	8										
Virtex2p		8	8										
VirtexE		12	12										
Virtex4		6	5										
Virtex5		8											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		33											
ProAsic3		10											
ProAsic3E		7											
Fusion		7											
EC		20											
ECP		20											
ECP2		6	5										
ECP2M		6	5										
SC		6	5										
MACHXO		6	5										
XP		6	5										
XP2		6	5										

## ADSU4B

### 4-Bit Cascadable Full Adder/Subtractor with Signed and Unsigned Operations, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			13										
Cyclone		24	24										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		24	24										
Stratix2		11	11										
Stratix3			13										
StratixGX		24	24										
Stratix2GX			10										
Max2		12	12										
Max3000a	33	33											
Max7000b	33	33											
Max7000ae	33	33											
Max7000s	33	33											
Spartan2		22	15										
Spartan2E		22	15										
Spartan3		18	17										
Spartan3A		14	13										
Spartan3ADSP		14	13										
Spartan3AN		14	13										
Spartan3E		8	8										
Spartan3L		14	13										
Virtex		22	15										
Virtex2		18	17										
Virtex2p		18	17										
VirtexE		22	15										
Virtex4		8	7										
Virtex5		14											
CoolRunner2	14												
CoolRunnerXpla3	14												
Xc9500	15												
Xc9500XL	15												
Xc9500XV	15												
ProAsicPlus		59											
ProAsic3	16												
ProAsic3E	13												
Fusion	13												
EC	30												
ECP	30												
ECP2	16	11											
ECP2M	16	11											
SC	18	12											
MACHXO	14	14											
XP	20	13											
XP2	12	9											

**FPGA Arithmetic Function Resource Usage**

**ADSU4S**

**4-Bit Cascadable Full Adder/Subtractor with Signed and Unsigned Operations,  
Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			13										
Cyclone		25	25										
Cyclone2		12	12										
Cyclone3		12	12										
Stratix		25	25										
Stratix2		11	11										
Stratix3			13										
StratixGX		25	25										
Stratix2GX			10										
Max2		12	12										
Max3000a	34	34											
Max7000b	34	34											
Max7000ae	34	34											
Max7000s	34	34											
Spartan2		22	21										
Spartan2E		22	21										
Spartan3		18	17										
Spartan3A		14	13										
Spartan3ADSP		14	13										
Spartan3AN		14	13										
Spartan3E		8	8										
Spartan3L		14	13										
Virtex		22	21										
Virtex2		18	17										
Virtex2p		18	17										
VirtexE		22	21										
Virtex4		8	7										
Virtex5		14											
CoolRunner2	15												
CoolRunnerXpla3	15												
Xc9500	19												
Xc9500XL	19												
Xc9500XV	19												
ProAsicPlus		59											
ProAsic3		16											
ProAsic3E		13											
Fusion		13											
EC		30											
ECP		30											
ECP2		16	11										
ECP2M		16	11										
SC		18	12										
MACHXO		14	14										
XP		20	13										
XP2		12	9										

**ADSU8B**

**8-Bit Cascadable Full Adder/Subtractor with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			25										
Cyclone		38	38										
Cyclone2		20	20										
Cyclone3		20	20										
Stratix		38	38										
Stratix2		19	19										
Stratix3			25										
StratixGX		38	38										
Stratix2GX			19										
Max2		20	20										
Max3000a	77	77											
Max7000b	77	77											
Max7000ae	77	77											
Max7000s	77	77											
Spartan2		38	27										
Spartan2E		38	27										
Spartan3		28	26										
Spartan3A		22	13										
Spartan3ADSP		22	13										
Spartan3AN		22	13										
Spartan3E		12	12										
Spartan3L		22	13										
Virtex		38	27										
Virtex2		28	26										
Virtex2p		28	26										
VirtexE		38	27										
Virtex4		12	11										
Virtex5		16											
CoolRunner2	32												
CoolRunnerXpla3	32												
Xc9500	33												
Xc9500XL	33												
Xc9500XV	33												
ProAsicPlus		115											
ProAsic3		28											
ProAsic3E		25											
Fusion		25											
EC		50											
ECP		50											
ECP2		20	15										
ECP2M		20	15										
SC		30	20										
MACHXO		26	23										
XP		32	21										
XP2		16	13										

**FPGA Arithmetic Function Resource Usage**

**ADSU16B**

**16-Bit Cascadable Full Adder/Subtractor with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			49										
Cyclone		70	70										
Cyclone2		36	36										
Cyclone3		36	36										
Stratix		70	70										
Stratix2		35	35										
Stratix3			49										
StratixGX		70	70										
Stratix2GX			35										
Max2		36	36										
Max3000a	163	163											
Max7000b	163	163											
Max7000ae	163	163											
Max7000s	163	163											
Spartan2		70	51										
Spartan2E		70	51										
Spartan3		52	50										
Spartan3A		38	21										
Spartan3ADSP		38	21										
Spartan3AN		38	21										
Spartan3E		20	20										
Spartan3L		38	21										
Virtex		70	51										
Virtex2		52	50										
Virtex2p		52	50										
VirtexE		70	51										
Virtex4		20	19										
Virtex5		24											
CoolRunner2	70												
CoolRunnerXpla3	66												
Xc9500	64												
Xc9500XL	64												
Xc9500XV	64												
ProAsicPlus		231											
ProAsic3		53											
ProAsic3E		50											
Fusion		49											
EC		90											
ECP		90											
ECP2		28	23										
ECP2M		28	23										
SC		54	36										
MACHXO		42	39										
XP		56	37										
XP2		24	21										

**ADSU32B**

**32-Bit Cascadable Full Adder/Subtractor with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			97										
Cyclone		134	134										
Cyclone2		68	68										
Cyclone3		68	68										
Stratix		134	134										
Stratix2		67	67										
Stratix3			97										
StratixGX		134	134										
Stratix2GX			67										
Max2		68	68										
Max3000a	343	343											
Max7000b	343	343											
Max7000ae	343	343											
Max7000s	267	267											
Spartan2		134	99										
Spartan2E		134	99										
Spartan3		100	98										
Spartan3A		70	37										
Spartan3ADSP		70	37										
Spartan3AN		70	37										
Spartan3E		36	36										
Spartan3L		70	37										
Virtex		134	99										
Virtex2		100	98										
Virtex2p		100	98										
VirtexE		134	99										
Virtex4		36	35										
Virtex5		40											
CoolRunner2	141												
CoolRunnerXpla3	524												
Xc9500	140												
Xc9500XL													
Xc9500XV	135												
ProAsicPlus		467											
ProAsic3		102											
ProAsic3E		99											
Fusion		102											
EC		170											
ECP		170											
ECP2		44	39										
ECP2M		44	39										
SC		102	68										
MACHXO		74	71										
XP		104	69										
XP2		40	37										

FPGA Arithmetic Function Resource Usage

ADSUR1

1-Bit Cascadable Registered Full Adder/Subtractor

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			2	2									
Cyclone		2	2	2									1
Cyclone2		2	2	2									
Cyclone3		2	2	2									
Stratix		2	2	2									1
Stratix2		4	4	2									
Stratix3			2	2									1
StratixGX		2	2	2									1
Stratix2GX			2	2									1
Max2		2	2	2									1
Max3000a	2	2		2									
Max7000b	2	2		2									
Max7000ae	2	2		2									
Max7000s	2	2		2									
Spartan2		6	5	2									
Spartan2E		6	5	2									
Spartan3		6	5	2									
Spartan3A		6	5	2									
Spartan3ADSP		6	5										
Spartan3AN		6	5										
Spartan3E		6	5	2									
Spartan3L		6	5	2									
Virtex		6	5	2									
Virtex2		6	5	2									
Virtex2p		6	5	2									
VirtexE		6	5	2									
Virtex4		6	5	2									
Virtex5		4	2	2									
CoolRunner2	2			2									
CoolRunnerXpla3	2			2									
Xc9500	2			2									
Xc9500XL	2			2									
Xc9500XV	2			2									
ProAsicPlus		14											
ProAsic3		7											
ProAsic3E		7											
Fusion		5											
EC		4		2									
ECP		4		2									
ECP2		4	2	2									
ECP2M		4	2	2									
SC		4	2	2									
MACHXO		4	2										
XP		4	2	2									
XP2		4	3	2									



## ADSUR2B

### 2-Bit Cascadable Registered Full Adder/Subtractor with Signed and Unsigned Operations, Bus Version

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6	4									
Cyclone		7	7	4							1	
Cyclone2		6	6	4								
Cyclone3		10	10	4								
Stratix		7	7	4							1	
Stratix2		8	8	4								
Stratix3			8	4							1	
StratixGX		7	7	4								
Stratix2GX			6	4							1	
Max2		6	6	4							1	
Max3000a	10	10		4								
Max7000b	10	10		4								
Max7000ae	10	10		4								
Max7000s	10	10		4								
Spartan2		16	16	4								
Spartan2E		16	16	4								
Spartan3		14	14	4								
Spartan3A		16	15	4								
Spartan3ADSP		16	15									
Spartan3AN		16	15									
Spartan3E		16	14	4								
Spartan3L		16	15	4								
Virtex		16	16	4								
Virtex2		14	14	4								
Virtex2p		14	14	4								
VirtexE		16	16	4								
Virtex4		18	16	4								
Virtex5		10	4	4								
CoolRunner2	4			4								
CoolRunnerXpla3	4			4								
Xc9500	4			4								
Xc9500XL	4			4								
Xc9500XV	4			4								
ProAsicPlus		36										
ProAsic3		24										
ProAsic3E		20										
Fusion		14										
EC		12		4								
ECP		12		4								
ECP2		10	9	4								
ECP2M		10	9	4								
SC		10	9	4								
MACHXO		10	9									
XP		10	9	4								
XP2		10	9	4								

**FPGA Arithmetic Function Resource Usage**

**ADSUR2S**

**2-Bit Cascadable Registered Full Adder/Subtractor with Signed and Unsigned Operations, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements 4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx		6	4									
Cyclone		7	7	4							1	
Cyclone2		6	6	4								
Cyclone3		10	10	4								
Stratix		7	7	4							1	
Stratix2		8	8	4								
Stratix3			8	4							1	
StratixGX		7	7	4							1	
Stratix2GX		6	4								1	
Max2		6	6	4							1	
Max3000a	11	11		4								
Max7000b	11	11		4								
Max7000ae	11	11		4								
Max7000s	11	11		4								
Spartan2		18	17	4								
Spartan2E		18	17	4								
Spartan3		14	14	4								
Spartan3A		16	15	4								
Spartan3ADSP		16	15									
Spartan3AN		16	15									
Spartan3E		16	14	4								
Spartan3L		16	15	4								
Virtex		18	17	4								
Virtex2		14	14	4								
Virtex2p		14	14	4								
VirtexE		18	17	4								
Virtex4		18	16	4								
Virtex5		12	4	4								
CoolRunner2	4			4								
CoolRunnerXpla3	4			4								
Xc9500	4			4								
Xc9500XL	4			4								
Xc9500XV	4			4								
ProAsicPlus		36										
ProAsic3		25										
ProAsic3E		20										
Fusion		14										
EC		12		4								
ECP		12		4								
ECP2		10	9	4								
ECP2M		10	9	4								
SC		10	9	4								
MACHXO		10	9									
XP		10	9	4								
XP2		10	9	4								

## ADSUR4B

### 4-Bit Cascadable Registered Full Adder/Subtractor with Signed and Unsigned Operations, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			18	6									
Cyclone		24	24	6									1
Cyclone2		19	19	6									
Cyclone3		14	14	6									
Stratix		24	24	6									1
Stratix2		17	17	6									
Stratix3			18	6									1
StratixGX		24	24	6									
Stratix2GX			17	6									1
Max2		19	19	6									1
Max3000a	28	28		6									
Max7000b	28	28		6									
Max7000ae	28	28		6									
Max7000s	28	28		6									
Spartan2		30	22	6									
Spartan2E		30	22	6									
Spartan3		26	24	6									
Spartan3A		28	26	6									
Spartan3ADSP		26	25										
Spartan3AN		28	26										
Spartan3E		24	22	6									
Spartan3L		26	25	6									
Virtex		30	22	6									
Virtex2		26	24	6									
Virtex2p		26	24	6									
VirtexE		30	22	6									
Virtex4		24	24	6									
Virtex5		18	6	6									
CoolRunner2	14			6									
CoolRunnerXpla3	14			6									
Xc9500	11			6									
Xc9500XL	11			6									
Xc9500XV	11			6									
ProAsicPlus		64											
ProAsic3		39											
ProAsic3E		32											
Fusion		24											
EC		38		6									
ECP		38		6									
ECP2		28	21	6									
ECP2M		28	21	6									
SC		22	17	6									
MACHXO		24	22										
XP		24	18	6									
XP2		26	20	6									

**FPGA Arithmetic Function Resource Usage**

**ADSUR4S**

**4-Bit Cascadable Registered Full Adder/Subtractor with Signed and Unsigned Operations, Single Pin Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			18	6									
Cyclone		26	26	6									1
Cyclone2		19	19	6									
Cyclone3		14	14	6									
Stratix		26	26	6									1
Stratix2		17	17	6									
Stratix3			18	6									1
StratixGX		26	26	6									1
Stratix2GX			17	6									1
Max2		19	19	6									1
Max3000a	29	29		6									
Max7000b	29	29		6									
Max7000ae	29	29		6									
Max7000s	29	29		6									
Spartan2		30	28	6									
Spartan2E		30	28	6									
Spartan3		26	24	6									
Spartan3A		28	26	6									
Spartan3ADSP		26	25										
Spartan3AN		28	26										
Spartan3E		24	22	6									
Spartan3L		26	25	6									
Virtex		30	28	6									
Virtex2		26	24	6									
Virtex2p		26	24	6									
VirtexE		30	28	6									
Virtex4		24	24	6									
Virtex5		22	6	6									
CoolRunner2	14			6									
CoolRunnerXpla3	14			6									
Xc9500	15			6									
Xc9500XL	15			6									
Xc9500XV	15			6									
ProAsicPlus		64											
ProAsic3		39											
ProAsic3E		32											
Fusion		24											
EC		38		6									
ECP		38		6									
ECP2		28	21	6									
ECP2M		28	21	6									
SC		22	17	6									
MACHXO		24	22										
XP		24	18	6									
XP2		26	20	6									

## ADSUR8B

### 8-Bit Cascadable Registered Full Adder/Subtractor with Signed and Unsigned Operations, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			34	10									
Cyclone		39	39	10								1	
Cyclone2		31	31	10									
Cyclone3		22	22	10									
Stratix		39	39	10								1	
Stratix2		29	29	10									
Stratix3			34	10								1	
StratixGX		39	39	10								1	
Stratix2GX			23	10								1	
Max2		31	31	10								1	
Max3000a	71	71		10									
Max7000b	71	71		10									
Max7000ae	71	71		10									
Max7000s	71	71		10									
Spartan2		50	38	10									
Spartan2E		50	38	10									
Spartan3		40	37	10									
Spartan3A		50	40	10									
Spartan3ADSP		48	39										
Spartan3AN		50	40										
Spartan3E		40	38	10									
Spartan3L		48	39	10									
Virtex		50	38	10									
Virtex2		40	37	10									
Virtex2p		40	37	10									
VirtexE		50	38	10									
Virtex4		40	37	10									
Virtex5		40	10	10									
CoolRunner2	31			10									
CoolRunnerXpla3	31			10									
Xc9500	32			10									
Xc9500XL	32			10									
Xc9500XV	32			10									
ProAsicPlus		124											
ProAsic3		67											
ProAsic3E		56											
Fusion		44											
EC		62		10									
ECP		62		10									
ECP2		44	33	10									
ECP2M		44	33	10									
SC		38	29	10									
MACHXO		50	40										
XP		40	30	10									
XP2		42	32	10									

**FPGA Arithmetic Function Resource Usage**

**ADSUR16B**

**16-Bit Cascadable Registered Full Adder/Subtractor with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			66	18									
Cyclone		71	71	18									1
Cyclone2		55	55	18									
Cyclone3		38	38	18									
Stratix		71	71	18									1
Stratix2		53	53	18									
Stratix3			66	18									1
StratixGX		71	71	18									1
Stratix2GX			39	18									1
Max2		55	55	18									1
Max3000a	155	155		18									
Max7000b	155	155		18									
Max7000ae	155	155		18									
Max7000s	155	155		18									
Spartan2		90	70	18									
Spartan2E		90	70	18									
Spartan3		72	69	18									
Spartan3A		90	72	18									
Spartan3ADSP		88	71										
Spartan3AN		90	72										
Spartan3E		72	70	18									
Spartan3L		88	71	18									
Virtex		90	70	18									
Virtex2		72	69	18									
Virtex2p		72	69	18									
VirtexE		90	70	18									
Virtex4		72	69	18									
Virtex5		68	18	18									
CoolRunner2	79			18									
CoolRunnerXpla3	73			18									
Xc9500	62			18									
Xc9500XL	62			18									
Xc9500XV	62			18									
ProAsicPlus		248											
ProAsic3		124											
ProAsic3E		106											
Fusion		84											
EC		110		18									
ECP		110		18									
ECP2		76	57	18									
ECP2M		76	57	18									
SC		70	53	18									
MACHXO		90	72										
XP		72	54	18									
XP2		74	56	18									

**ADSUR32B**

**32-Bit Cascadable Registered Full Adder/Subtractor with Signed and Unsigned Operations, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			130	34									
Cyclone		135	135	34									1
Cyclone2		103	103	34									
Cyclone3		70	70	34									
Stratix		135	135	34									1
Stratix2		101	101	34									
Stratix3			130	34									1
StratixGX		135	135	34									1
Stratix2GX			71	34									1
Max2		103	103	34									1
Max3000a	330	330		34									
Max7000b	330	330		34									
Max7000ae	330	330		34									
Max7000s	255	255		34									
Spartan2		170	134	34									
Spartan2E		170	134	34									
Spartan3		136	133	34									
Spartan3A		170	136	34									
Spartan3ADSP		168	135										
Spartan3AN		170	136										
Spartan3E		136	134	34									
Spartan3L		168	135	34									
Virtex		170	134	34									
Virtex2		136	133	34									
Virtex2p		136	133	34									
VirtexE		170	134	34									
Virtex4		136	133	34									
Virtex5		140	34	34									
CoolRunner2	148			34									
CoolRunnerXpla3	528			34									
Xc9500	137			34									
Xc9500XL													
Xc9500XV	132			34									
ProAsicPlus		500											
ProAsic3		254											
ProAsic3E		206											
Fusion		164											
EC		206		34									
ECP		206		34									
ECP2		140	105	34									
ECP2M		140	105	34									
SC		134	101	34									
MACHXO		170	136										
XP		136	102	34									
XP2		138	104	34									

FPGA Arithmetic Function Resource Usage

**MULT2B**

**2x2 Signed Multiplier, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			4										
StratixGX		4	4										
Stratix2GX			4										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		8	7										
Spartan2E		8	7										
Spartan3		8	7										
Spartan3A		8	8										
Spartan3ADSP		8	7										
Spartan3AN		8	7										
Spartan3E		8	7										
Spartan3L		8	7										
Virtex		8	7										
Virtex2		8	7										
Virtex2p		8	7										
VirtexE		8	7										
Virtex4		8	7										
Virtex5		6											
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		25											
ProAsic3		18											
ProAsic3E		18											
Fusion		18											
EC		6	4										
ECP		6	4										
ECP2		10	8										
ECP2M		10	8										
SC		8	7										
MACHXO		8	7										
XP		4	4										
XP2		10	8										



## MULT2S

### 2x2 Signed Multiplier, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4										
Cyclone		4	4										
Cyclone2		4	4										
Cyclone3		4	4										
Stratix		4	4										
Stratix2		4	4										
Stratix3			4										
StratixGX		4	4										
Stratix2GX			4										
Max2		4	4										
Max3000a	4	4											
Max7000b	4	4											
Max7000ae	4	4											
Max7000s	4	4											
Spartan2		8	7										
Spartan2E		8	7										
Spartan3		8	7										
Spartan3A		8	8										
Spartan3ADSP		8	7										
Spartan3AN		8	7										
Spartan3E		8	7										
Spartan3L		8	7										
Virtex		8	7										
Virtex2		8	7										
Virtex2p		8	7										
VirtexE		8	7										
Virtex4		8	7										
Virtex5			6										
CoolRunner2	4												
CoolRunnerXpla3	4												
Xc9500	4												
Xc9500XL	4												
Xc9500XV	4												
ProAsicPlus		25											
ProAsic3		18											
ProAsic3E		18											
Fusion		18											
EC		4	4										
ECP		4	4										
ECP2		10	8										
ECP2M		10	8										
SC		8	7										
MACHXO		8	7										
XP		4	4										
XP2		10	8										

**FPGA Arithmetic Function Resource Usage**

**MULT4B**

**4x4 Signed Multiplier, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx									1				
Cyclone		30	30										
Cyclone2									1				
Cyclone3									1				
Stratix									1				
Stratix2									1				
Stratix3													
StratixGX									1				
Stratix2GX									1				
Max2		31	31										
Max3000a		34	34										
Max7000b		34	34										
Max7000ae		34	34										
Max7000s		34	34										
Spartan2			24	20									
Spartan2E			24	20									
Spartan3									1				
Spartan3A									1				
Spartan3ADSP													
Spartan3AN									1				
Spartan3E									1				
Spartan3L													
Virtex		24	20										
Virtex2									1				
Virtex2p									1				
VirtexE		24	20										
Virtex4									1				
Virtex5		18											
CoolRunner2		27											
CoolRunnerXpla3													
Xc9500		29											
Xc9500XL		29											
Xc9500XV		29											
ProAsicPlus		101											
ProAsic3		64											
ProAsic3E		64											
Fusion		59											
EC		68	49										
ECP									1				
ECP2													
ECP2M													
SC		68	49										
MACHXO		44	37										
XP		68	49										
XP2													

## MULT4S

### 4x4 Signed Multiplier, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx									1				
Cyclone		30	30										
Cyclone2									1				
Cyclone3									1				
Stratix									1				
Stratix2									1				
Stratix3													
StratixGX									1				
Stratix2GX									1				
Max2		31	31										
Max3000a		34	34										
Max7000b		34	34										
Max7000ae		34	34										
Max7000s		34	34										
Spartan2			24	20									
Spartan2E			24	20									
Spartan3									1				
Spartan3A									1				
Spartan3ADSP													
Spartan3AN									1				
Spartan3E									1				
Spartan3L													
Virtex		24	20										
Virtex2									1				
Virtex2p									1				
VirtexE		24	20										
Virtex4									1				
Virtex5		16											
CoolRunner2		27											
CoolRunnerXpla3		31											
Xc9500		29											
Xc9500XL		29											
Xc9500XV		29											
ProAsicPlus			101										
ProAsic3			64										
ProAsic3E			64										
Fusion			60										
EC			68	49									
ECP									1				
ECP2													
ECP2M													
SC			68	49									
MACHXO			44	37									
XP			68	49									
XP2													

FPGA Arithmetic Function Resource Usage

**MULT8B**

**8x8 Signed Multiplier, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx								1				
Cyclone		134	134									
Cyclone2								1				
Cyclone3								1				
Stratix								1				
Stratix2								1				
Stratix3												
StratixGX								1				
Stratix2GX								1				
Max2		135	135									
Max3000a	363	363										
Max7000b	363	363										
Max7000ae	363	363										
Max7000s	238	238										
Spartan2		78	68									
Spartan2E		78	68									
Spartan3								1				
Spartan3A								1				
Spartan3ADSP								1				
Spartan3AN								1				
Spartan3E								1				
Spartan3L												
Virtex		78	68									
Virtex2								1				
Virtex2p								1				
VirtexE		78	68									
Virtex4								1				
Virtex5								1				
CoolRunner2	120											
CoolRunnerXpla3	120											
Xc9500	152											
Xc9500XL	152											
Xc9500XV	152											
ProAsicPlus		412										
ProAsic3		300										
ProAsic3E		303										
Fusion		299										
EC		242	175									
ECP								1				
ECP2												
ECP2M												
SC		242	175									
MACHXO		174	140									
XP		242	175									
XP2												

## MULT16B

### 16x16 Signed Multiplier, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx									2				
Cyclone		396	396										
Cyclone2									2				
Cyclone3									2				
Stratix									2				
Stratix2									2				
Stratix3													
StratixGX									2				
Stratix2GX									2				
Max2		396	396										
Max3000a	995	995											
Max7000b	995	995											
Max7000ae	995	995											
Max7000s	995	995											
Spartan2		286	262										
Spartan2E		286	262										
Spartan3									1				
Spartan3A									1				
Spartan3ADSP									1				
Spartan3AN									1				
Spartan3E									1				
Spartan3L													
Virtex		286	262										
Virtex2									1				
Virtex2p									1				
VirtexE		286	262										
Virtex4									1				
Virtex5									1				
CoolRunner2	501												
CoolRunnerXpla3	450												
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus		1330											
ProAsic3		1008											
ProAsic3E		1014											
Fusion		969											
EC		930	671										
ECP									1				
ECP2													
ECP2M													
SC		930	671										
MACHXO		770	598										
XP		930	671										
XP2													

**FPGA Arithmetic Function Resource Usage**

**MULT18B**

**18x18 Signed Multiplier, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx									2				
Cyclone		490	490										
Cyclone2									2				
Cyclone3									2				
Stratix									2				
Stratix2									2				
Stratix3													
StratixGX									2				
Stratix2GX									2				
Max2		490	490										
Max3000a	1239	1239											
Max7000b	1239	1239											
Max7000ae	1239	1239											
Max7000s	1239	1239											
Spartan2		370	326										
Spartan2E		370	326										
Spartan3									1				
Spartan3A									1				
Spartan3ADSP									1				
Spartan3AN									1				
Spartan3E									1				
Spartan3L													
Virtex		370	326										
Virtex2									1				
Virtex2p									1				
VirtexE		370	326										
Virtex4									1				
Virtex5									1				
CoolRunner2	2566												
CoolRunnerXpla3	2566												
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus		1628											
ProAsic3		1230											
ProAsic3E		1238											
Fusion		1178											
EC		1172	845										
ECP									1				
ECP2													
ECP2M													
SC		1172	845										
MACHXO		986	755										
XP		1172	845										
XP2													

## MULT32B

### 32x32 Signed Multiplier, Bus Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx									8				
Cyclone		1428	1428										
Cyclone2		107	107						8				
Cyclone3		108	108						8				
Stratix									8				
Stratix2									8				
Stratix3													
StratixGX									8				
Stratix2GX									8				
Max2		1428	1428										
Max3000a													
Max7000b													
Max7000ae													
Max7000s													
Spartan2		1096	1036										
Spartan2E		1096	1036										
Spartan3		86	80						4				
Spartan3A		492	444						3				
Spartan3ADSP		48	47						4				
Spartan3AN		492	444						3				
Spartan3E		82	80						4				
Spartan3L		82	80										
Virtex		1096	1036										
Virtex2		86	80						4				
Virtex2p		86	80						4				
VirtexE		1096	1036										
Virtex4									4				
Virtex5									4				
CoolRunner2													
CoolRunnerXpla3													
Xc9500													
Xc9500XL													
Xc9500XV													
ProAsicPlus		4691											
ProAsic3		3356											
ProAsic3E		3402											
Fusion													
EC		3660	2633										
ECP									1				
ECP2													
ECP2M													
SC		3660	2633										
MACHXO		2272	2260										
XP		3660	2633										
XP2													

FPGA Arithmetic Function Resource Usage

**MULTR2B**

**2x2 Signed Registered Multiplier, Bus Version**

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4									1
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4									1
Stratix2		4	4	4									
Stratix3			4	4									1
StratixGX		4	4	4									1
Stratix2GX			4	4									1
Max2		4	4	4									1
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		12	11	4									
Spartan2E		12	11	4									
Spartan3		12	11	4									
Spartan3A		12	12	4									
Spartan3ADSP		12	11										
Spartan3AN		12	11										
Spartan3E		12	11	4									
Spartan3L		12	11	4									
Virtex		12	11	4									
Virtex2		12	11	4									
Virtex2p		12	11	4									
VirtexE		12	11	4									
Virtex4		12	11	4									
Virtex5		10	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		29											
ProAsic3		22											
ProAsic3E		22											
Fusion		18											
EC		8	4	4									
ECP		8	4	4									
ECP2		8	8	4									
ECP2M		8	8	4									
SC		8	7	4									
MACHXO		8	7										
XP		8	4	4									
XP2		8	8	4									



## MULTR2S

### 2x2 Signed Registered Multiplier, Single Pin Version

Device Family	Macrocells	Logic Cells/Elements	4-Input LUT	Registers	Block RAM (16K-Bit)	Block RAM (4K-Bit)	Block RAM (8Kx18)	Block RAM (256x9)	Block Multipliers	Total PLLs	Total DLLs	D/GCLK	DCMs
Arriagx			4	4									
Cyclone		4	4	4									1
Cyclone2		4	4	4									
Cyclone3		4	4	4									
Stratix		4	4	4									1
Stratix2		4	4	4									
Stratix3			4	4									1
StratixGX		4	4	4									1
Stratix2GX			4	4									1
Max2		4	4	4									1
Max3000a	4	4		4									
Max7000b	4	4		4									
Max7000ae	4	4		4									
Max7000s	4	4		4									
Spartan2		12	11	4									
Spartan2E		12	11	4									
Spartan3		12	11	4									
Spartan3A		12	12	4									
Spartan3ADSP		12	11										
Spartan3AN		12	11										
Spartan3E		12	11	4									
Spartan3L		12	11	4									
Virtex		12	11	4									
Virtex2		12	11	4									
Virtex2p		12	11	4									
VirtexE		12	11	4									
Virtex4		12	11	4									
Virtex5		10	4	4									
CoolRunner2	4			4									
CoolRunnerXpla3	4			4									
Xc9500	4			4									
Xc9500XL	4			4									
Xc9500XV	4			4									
ProAsicPlus		29											
ProAsic3		22											
ProAsic3E		22											
Fusion		18											
EC		8	4	4									
ECP		8	4	4									
ECP2		8	8	4									
ECP2M		8	8	4									
SC		8	7	4									
MACHXO		8	7										
XP		8	4	4									
XP2		8	8	4									

























































