PRTx Parallel Port Unit

Summary

This document provides detailed reference information with respect to the parallel port unit peripheral device.

Core Reference
CR0108 (v2.0) March 13, 2008

The PRTx Parallel Port Unit is simply a register interface for storing data to be transferred to/from another device in a design. For example, when used with a microcontroller such as the TSK80x, which does not have any on-core port interfaces, the unit provides a valuable new extension to the processor's feature set.

Available Devices

The PRTx family of devices can be further divided into the following three sub-families

- **PRTOx** – output only port devices
- **PRTIOx** – I/O port devices
- **PRTIOXx** – I/O port devices with additional tristate buffer enable output for each port.

Within each sub-family single, two and four port devices with 8 or 32-bit port widths are available – each of which are standard, non-Wishbone variants.

All devices can be found in the FPGA Peripherals integrated library (`FPGA Peripherals.IntLib`), located in the `\Library\Fpga` folder of the installation.

Functional Description

PRTOx

Symbols

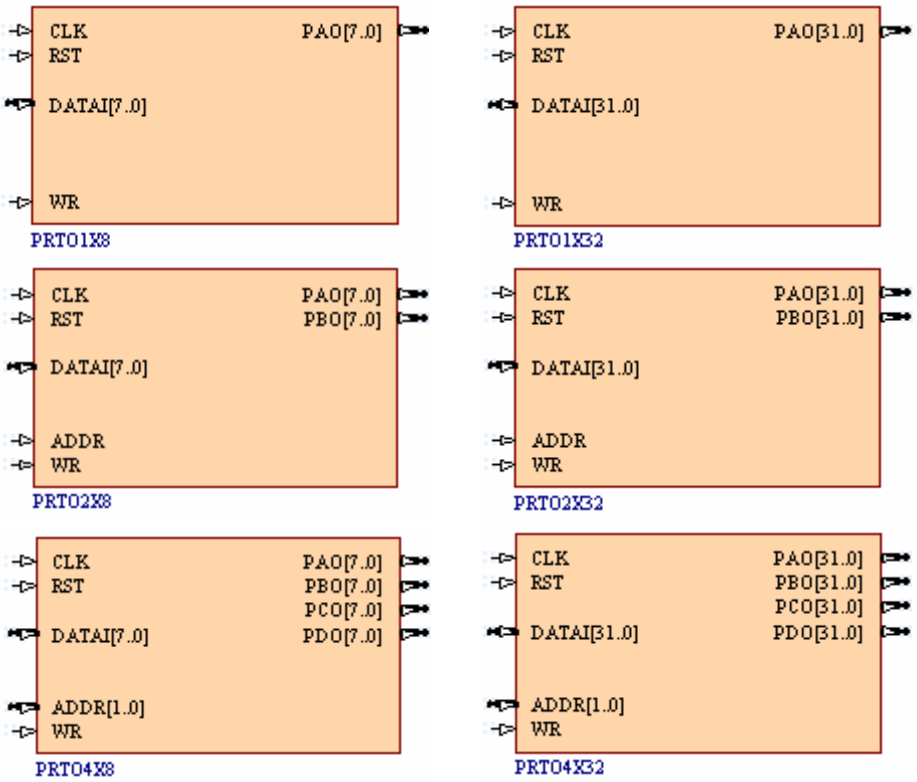

Figure 1. PRTOx family symbols

Pin Description

Table 1. PRTOx pin description

Name	Type	Polarity/ Bus size	Description
Control Signals			
CLK	I	Rise	External (System) Clock
RST	I	High	External (System) Reset
Peripheral Interface Signals			
DATAI	I	8/32	Data received from host peripheral device
ADDR[1]	I	1/2[2]	Address bus, used to select an internal register of the device for writing to.
WR	I	High	Write enable signal. When active, data can be written to an internal register of the device.

[1] The ADDR signal applies only to the PRTO2X8, PRTO2X32, PRTO4X8 and PRTO4X32 devices, where there are 2 and 4 internal registers that can be addressed, respectively.

[2] The number of address bits used in the ADDR signal depends on the number of ports that the device supports and hence the number of internal registers that can be addressed for writing. For the PRTO2X8 and PRTO2X32 devices, which provide two ports, there are two internal registers so the number of address bits required is 1. For the PRTO4X8 and PRTO4X32 devices, there are four internal registers and so 2 address bits are required.

Name	Type	Polarity/ Bus size	Description
Port Output Signals			
PAO	O	8/32	Port A output bus
PBO[3]	O	8/32	Port B output bus
PCO[4]	O	8/32	Port C output bus
PDO[4]	O	8/32	Port D output bus

PRTIOx

Symbols

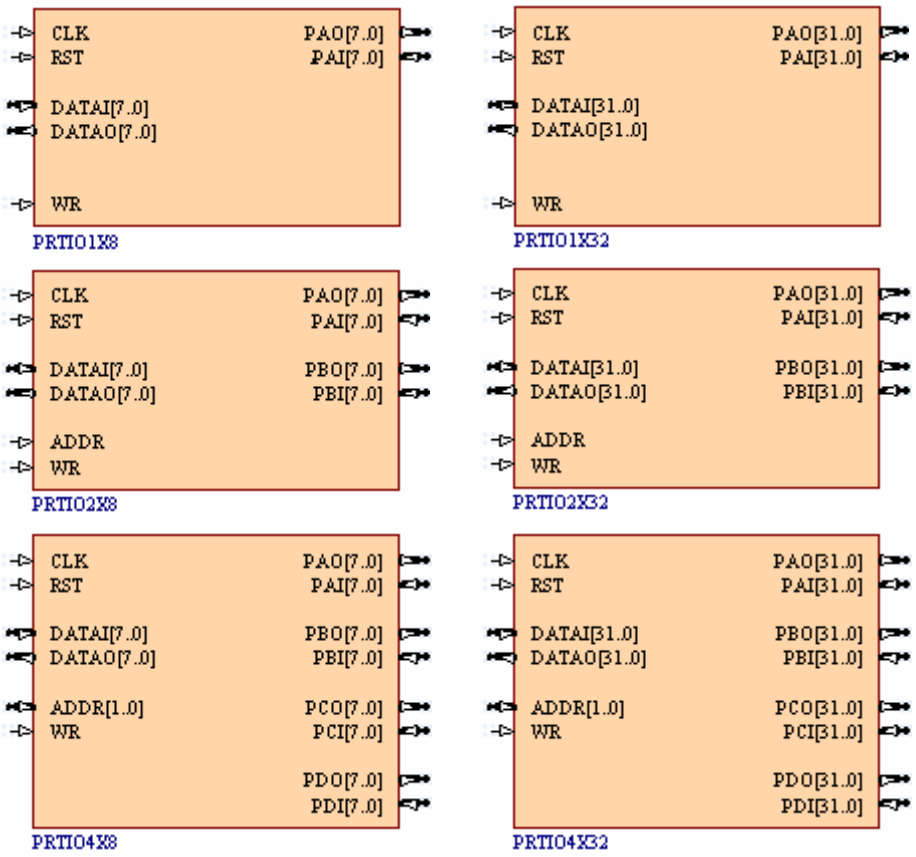

Figure 2. PRTIOx family symbols

[3] PRT02X8, PRTO2X32, PRTO4X8 and PRTO4X32 only.

[4] PRTO4X8 and PRTO4X32 only.

Pin Description

Table 2. PRTIOx pin description

Name	Type	Polarity/ Bus size	Description
Control Signals			
CLK	I	Rise	External (System) Clock
RST	I	High	External (System) Reset
Peripheral Interface Signals			
DATAI	I	8/32	Data received from host peripheral device
DATAO	O	8/32	Data to be sent to host peripheral device
ADDR[5]	I	1/2[6]	Address bus, used to select an internal register of the device for writing to.
WR	I	High	Write enable signal. When active, data can be written to an internal register of the device.
Port Input Signals			
PAI	I	8/32	Port A input bus
PBI[7]	I	8/32	Port B input bus
PCI[8]	I	8/32	Port C input bus
PDI[8]	I	8/32	Port D input bus
Port Output Signals			
PAO	O	8/32	Port A output bus
PBO[7]	O	8/32	Port B output bus
PCO[8]	O	8/32	Port C output bus
PDO[8]	O	8/32	Port D output bus

[5] The ADDR signal applies only to the PRTIO2X8, PRTIO2X32, PRTIO4X8 and PRTIO4X32 devices, where there are 2 and 4 internal registers that can be addressed, respectively.

[6] The number of address bits used in the ADDR signal depends on the number of internal registers that can be addressed. For the PRTIO2X8 and PRTIO2X32 devices, there are two internal registers so the number of address bits required is 1. For the PRTIO4X8 and PRTIO4X32 devices, there are four internal registers and so 2 address bits are required.

[7] PRTIO2X8, PRTIO2X32, PRTIO4X8 and PRTIO4X32 only.

[8] PRTIO4X8 and PRTIO4X32 only.

PRTIOXx

Symbols

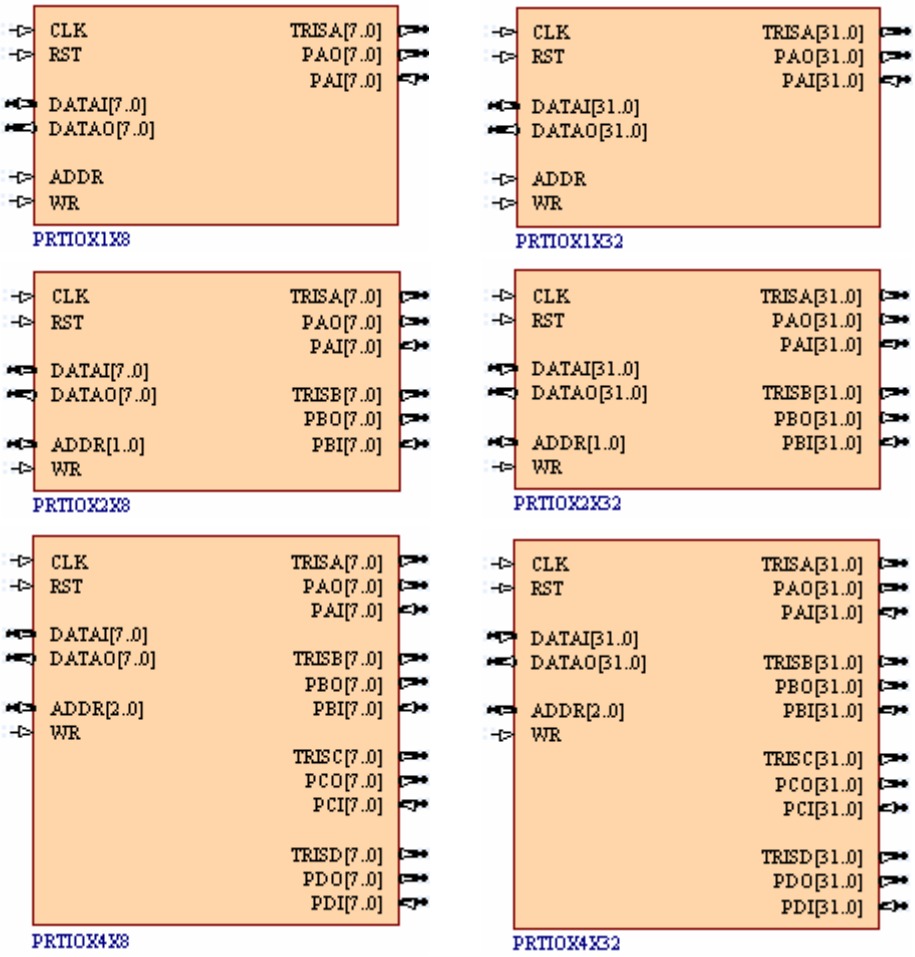

Figure 3. PRTIOXx family symbols

Pin Description

Table 3. PRTIOXx pin description

Name	Type	Polarity/ Bus size	Description
Control Signals			
CLK	I	Rise	External (System) Clock
RST	I	High	External (System) Reset
Peripheral Interface Signals			
DATAI	I	8/32	Data received from host peripheral device
DATAO	O	8/32	Data to be sent to host peripheral device
ADDR	I	1-3[9]	Address bus, used to select an internal register of the device for writing to.

[9] The number of address bits used in the ADDR signal depends on the number of internal registers that can be addressed. For the PRTIOX1X8 and PRTIOX1X32 devices, there are two internal registers so the number of address bits required is 1. For the PRTIOX2X8 and PRTIOX2X32 devices, there are four internal registers and so 2 address bits are required. For the PRTIOX4X8 and PRTIOX4X32 devices, there are eight internal registers and so 3 address bits are required.

Name	Type	Polarity/ Bus size	Description
WR	I	High	Write enable signal. When active, data can be written to an internal register of the device.
Port Input Signals			
PAI	I	8/32	Port A input bus
PBI[10]	I	8/32	Port B input bus
PCI[11]	I	8/32	Port C input bus
PDI[11]	I	8/32	Port D input bus
Port Output Signals			
PAO	O	8/32	Port A output bus
PBO[10]	O	8/32	Port B output bus
PCO[11]	O	8/32	Port C output bus
PDO[11]	O	8/32	Port D output bus
TRISA	O	8/32	External Tristate Buffer control output for Port A
TRISB[10]	O	8/32	External Tristate Buffer control output for Port B
TRISC[11]	O	8/32	External Tristate Buffer control output for Port C
TRISD[11]	O	8/32	External Tristate Buffer control output for Port D

Note: The TRIS registers are simple registers – there is no internal connection between these registers and their corresponding port registers. You could use the TRIS registers in a device as simple output only ports (used in the same way as the PRTOx devices). The TRIS registers can also be used to provide the control signal to external tristate buffers, when you wish to use a bidirectional bus.

[10] PRTIOX2X8, PRTIOX2X32, PRTIOX4X8 and PRTIOX4X32 only.

[11] PRTIOX4X8 and PRTIOX4X32 only.

Hardware Description

Block Diagrams

PRTOx Block Diagrams

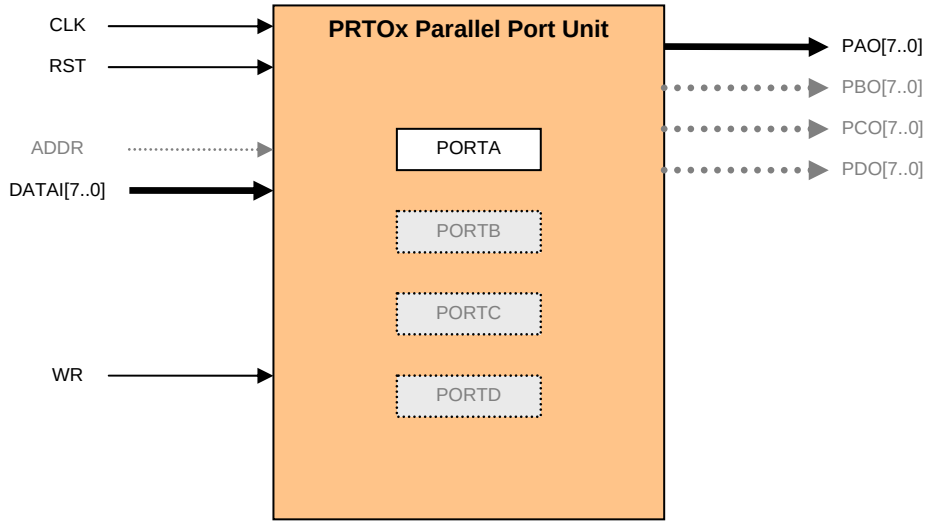

Figure 4. PRTOx Parallel Port Unit Block Diagram (8-bit data and port width).

Figure 4 is drawn primarily to represent the PRTO1X8 device. The grayed-out areas of the diagram apply to the PRTO2X8 and/or PRTO4X8 devices only.

Note: ADDR will be 1 bit for the PRTO2X8 and 2 bits for the PRTO4X8.

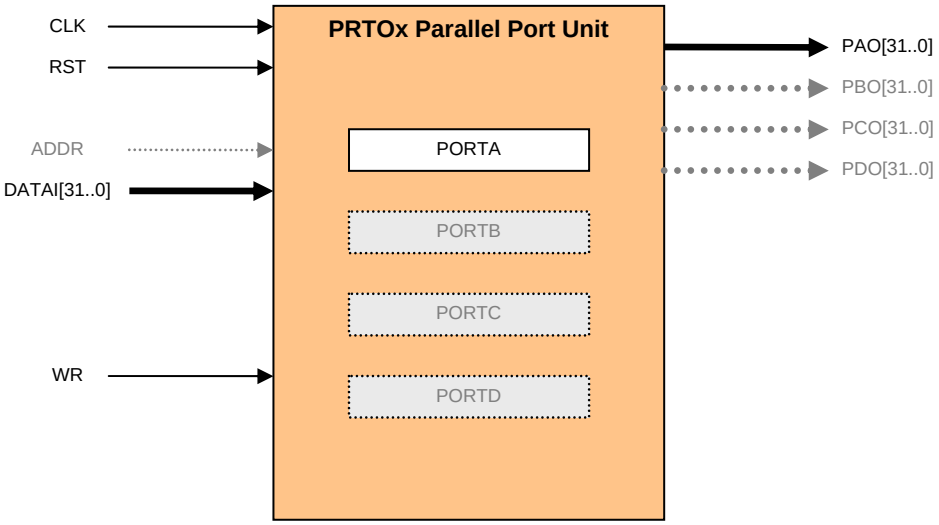

Figure 5. PRTOx Parallel Port Unit Block Diagram (32-bit data and port width).

Figure 5 is drawn primarily to represent the PRTO1X32 device. The grayed-out areas of the diagram apply to the PRTO2X32 and/or PRTO4X32 devices only.

Note: ADDR will be 1 bit for the PRTO2X32 and 2 bits for the PRTO4X32.

PRTIOx Block Diagrams

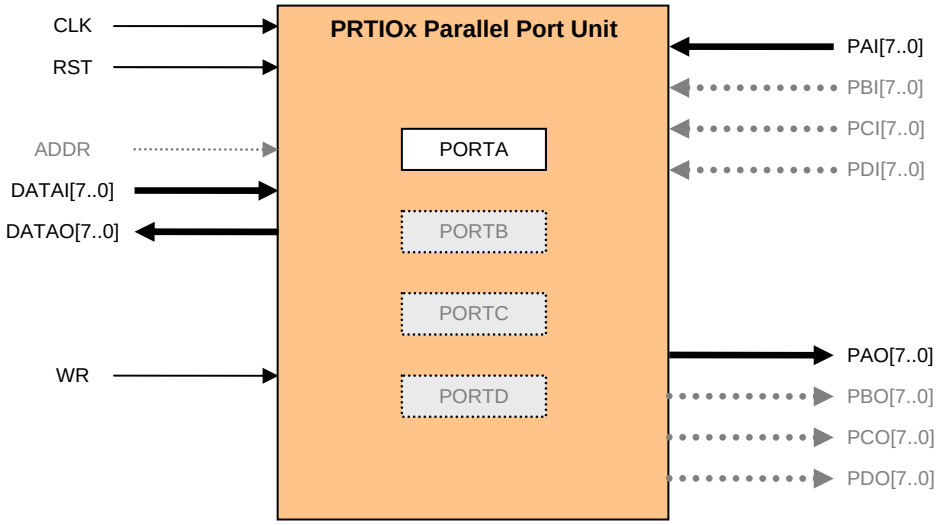

Figure 6. PRTIOx Parallel Port Unit Block Diagram (8-bit data and port width).

Figure 6 is drawn primarily to represent the PRTIO1X8 device. The grayed-out areas of the diagram apply to the PRTIO2X8 and/or PRTIO4X8 devices only.

Note: ADDR will be 1 bit for the PRTIO2X8 and 2 bits for the PRTIO4X8.

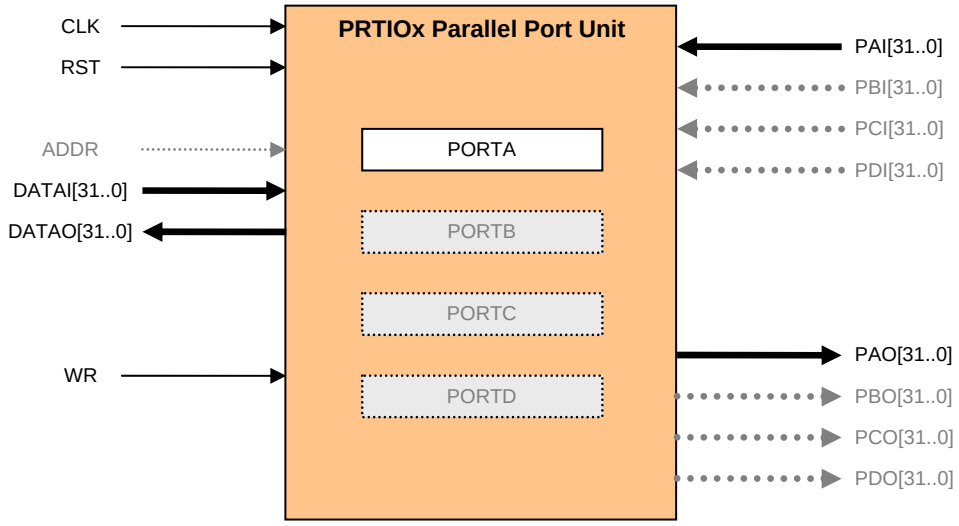

Figure 7. PRTIOx Parallel Port Unit Block Diagram (32-bit data and port width).

Figure 7 is drawn primarily to represent the PRTIO1X32 device. The grayed-out areas of the diagram apply to the PRTIO2X32 and/or PRTIO4X32 devices only.

Note: ADDR will be 1 bit for the PRTIO2X32 and 2 bits for the PRTIO4X32.

PRTIOXx Block Diagrams

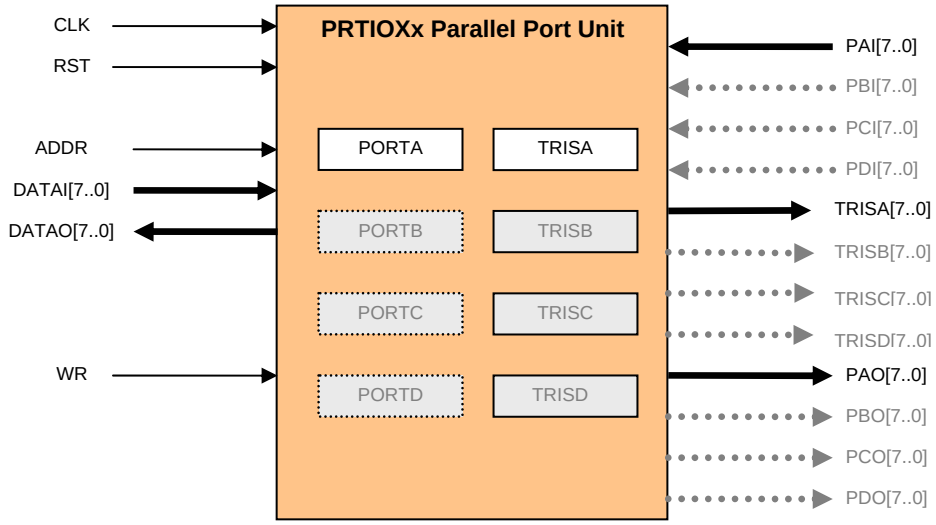

Figure 8. PRTIOXx Parallel Port Unit Block Diagram (8-bit data and port width).

Figure 8 is drawn primarily to represent the PRTIOX1X8 device. The grayed-out areas of the diagram apply to the PRTIOX2X8 and/or PRTIOX4X8 devices only.

Note: ADDR will be 1 bit for the PRTIOX1X8, 2 bits for the PRTIOX2X8 and 3 bits for the PRTIOX4X8.

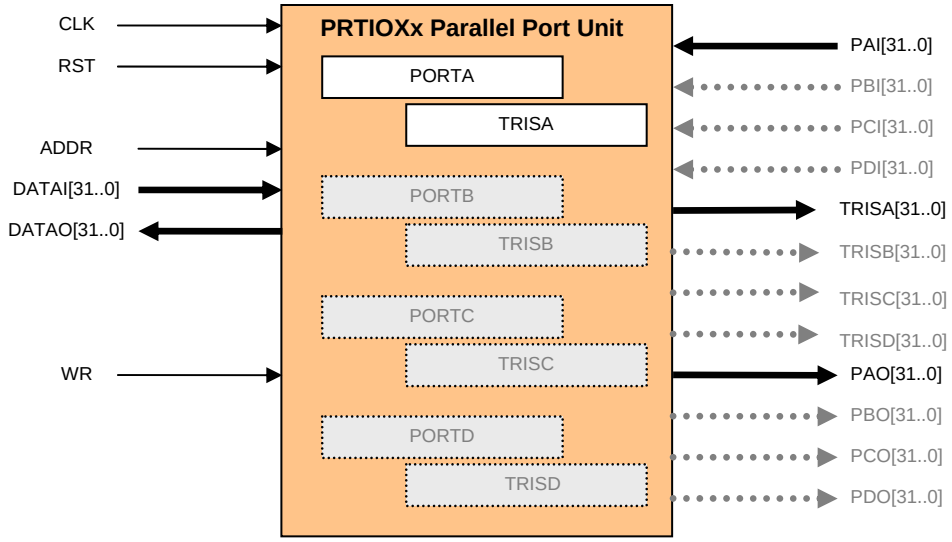

Figure 9. PRTIOXx Parallel Port Unit Block Diagram (32-bit data and port width).

Figure 9 is drawn primarily to represent the PRTIOX1X32 device. The grayed-out areas of the diagram apply to the PRTIOX2X32 and/or PRTIOX4X32 devices only.

Note: ADDR will be 1 bit for the PRTIOX1X32, 2 bits for the PRTIOX2X32 and 3 bits for the PRTIOX4X32.

Register Reset Values

Table 4 shows the values contained in each of the PRTx's internal registers after an external system reset has been received on the RST input.

Table 4. Register reset values

Register	Value after reset	
	8-bit port width	32-bit port width
PORTA	00h	0000h
PORTB	00h	0000h
PORTC	00h	0000h
PORTD	00h	0000h
TRISA	FFh	FFFFh
TRISB	FFh	FFFFh
TRISC	FFh	FFFFh
TRISD	FFh	FFFFh

Writing to the Internal Registers

The host peripheral device can write to any of the PRTx's internal registers. With respect to the PRTO1X8, PRTO1X32, PRTIO1X8 and PRTIO1X32 devices, there is only one internal register, so addressing is not required (and therefore no ADDR signal).

For all other devices in the family, which possess two or more internal registers, selection of a particular register is achieved by supplying the unique, binary ID address code of the register. This code is sent to the device and appears at the ADDR input.

Table 5 shows the unique address IDs associated with each of the registers for the PRTO2X8, PRTO2X32, PRTIO2X8 and PRTIO2X32 devices, which possess two internal registers.

Table 5. PRTO2X8, PRTO2X32, PRTIO2X8, PRTIO2X32 Internal register unique address IDs.

Register	Unique Register Address ID
PORTA	0
PORTB	1

Table 6 shows the unique address IDs for the registers within the PRTO4X8, PRTO4X32, PRTIO4X8 and PRTIO4X32 devices.

Table 6. PRTO4X8, PRTO4X32, PRTIO4X8, PRTIO4X32 Internal register unique address IDs.

Register	Unique Register Address ID
PORT A	00
PORT B	01
PORT C	10
PORT D	11

The PRTIOXx sub-family of devices are slightly different due to the presence of an additional TRIS register for each port. Tables 7-9 show the unique address IDs for the registers in the PRTIOX1X8/PRTIOX1X32, PRTIOX2X8/PRTIOX2X32 and PRTIOX4X8/PRTIOX4X32 respectively.

Table 7. PRTIOX1X8, PRTIOX1X32 Internal register unique address IDs.

Register	Unique Register Address ID
PORTA	0
TRISA	1

Table 8. PRTIOX2X8, PRTIOX2X32 Internal register unique address IDs.

Register	Unique Register Address ID
PORTA	00
PORTB	01
TRISA	10
TRISB	11

Table 9. PRTIOX4X8, PRTIOX4X32 Internal register unique address IDs.

Register	Unique Register Address ID
PORTA	000
PORTB	001
PORTC	010
PORTD	011
TRISA	100
TRISB	101
TRISC	110
TRISD	111

An internal register of the PRTx device can be written to in the following circumstances. In each case, the write operation occurs on the rising edge of the CLK input.

System Reset

After reception of an external system reset (RST goes High), each internal Port register is loaded with the reset value (00h for 8-bit port widths; 0000h for 32-bit port widths). For the PRTIOXx devices, the TRIS registers are loaded with the value FFh (for 8-bit port widths) or FFFFh (for 32-bit port widths).

Host Peripheral Write

The write operation occurs on the rising edge of the CLK input and can be summarized as follows:

- The host writes the unique address ID for the register to be written to the ADDR input of the PRTx device
- The host sends a valid byte of data to the PRTx's DATAI input
- The host then sets the PRTx's WR signal High, to specify a Write cycle
- The PRTx device latches the byte of data into the target register.

Reading Port Data

Data is read constantly from the PRTx device and directly from the relevant port input bus. The data is not read from an internal register as the incoming data on a port input line is not latched.

PRTOx devices provide output ports only and so data cannot be read using these devices.

For the PRTIO1X8 and PRTIO1X32 devices, as there is only one port, data will be read constantly from this port.

For devices with more than one port, the port input bus that is read depends on the unique address ID supplied to the ADDR input of the device.

If you are using a PRTIOXx device and do not specify a unique address ID on the ADDR line representing an internal port register (i.e. you specify the address of a TRIS register), the actual data read could be from any of the port input lines.

Revision History

Date	Version No.	Revision
29-Jan-2004	1.0	New product release
21-Sep-2004	1.1	Addition of Wishbone-compliant versions
04-Nov-2004	1.2	Addition of 32-bit versions
01-Dec-2004	1.3	Schematic symbol updates
13-Dec-2004	1.4	Removal of Wishbone-compliant versions. Wishbone-compliant parallel port devices can be placed in a design using the WB_PRTIO device. Refer to the *WB_PRTIO Configurable Wishbone Parallel Port Unit* core reference for further detail
26-May-2005	1.5	Updated for Altium Designer SP4
12-Dec-2005	1.6	Path references updated for Altium Designer 6
13-Mar-2008	2.0	Updated for Altium Designer Summer 08