MAX1104 DAC Controller

Summary

This document provides detailed reference information with respect to the MAX1104_DAC Controller peripheral device, which interfaces to the MAX1104 8-bit CODEC on Altium's NanoBoard-NB1.

The MAX1104_DAC Controller provides a simple interface to the MAX1104 8-bit CODEC device on the NanoBoard-NB1.

Note: Although the on-board MAX1104 CODEC device provides both an ADC and a DAC, only the DAC is used.

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Available Devices

The MAX1104_DAC device can be found in the FPGA Peripherals integrated library (`FPGA Peripherals.IntLib`), located in the `\Library\Fpga` folder of the installation.

Functional Description

Symbol

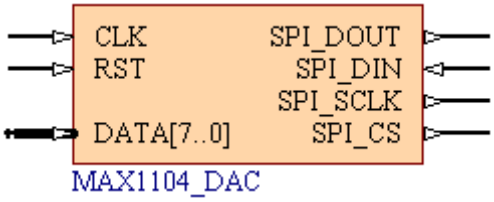

Figure 1. MAX1104_DAC Symbol

Pin Description

Table 1. MAX1104_DAC Pin description

Name	Type	Polarity/ Bus size	Description
Control Signals			
CLK	I	Rise	External clock signal
RST	I	High	Asynchronous external system reset
Host Interface Signals			
DATA	I	8	Data received from the host device (e.g. microcontroller, memory space), which is to be sent to the CODEC
CODEC Interface Signals			
SPI_DOUT	O	8	Serial Data Output. This is data sent to the CODEC device.

Name	Type	Polarity/ Bus size	Description
SPI_DIN	I	8	Serial Data Input. This is data received from the CODEC device.
SPI_SCLK1	O	Rise	Serial Clock. The frequency of this clock is half that of the external clock arriving at the CLK input.
SPI_CS	O	Low	Chip Select. When active, the CODEC device is enabled.

Block Diagram

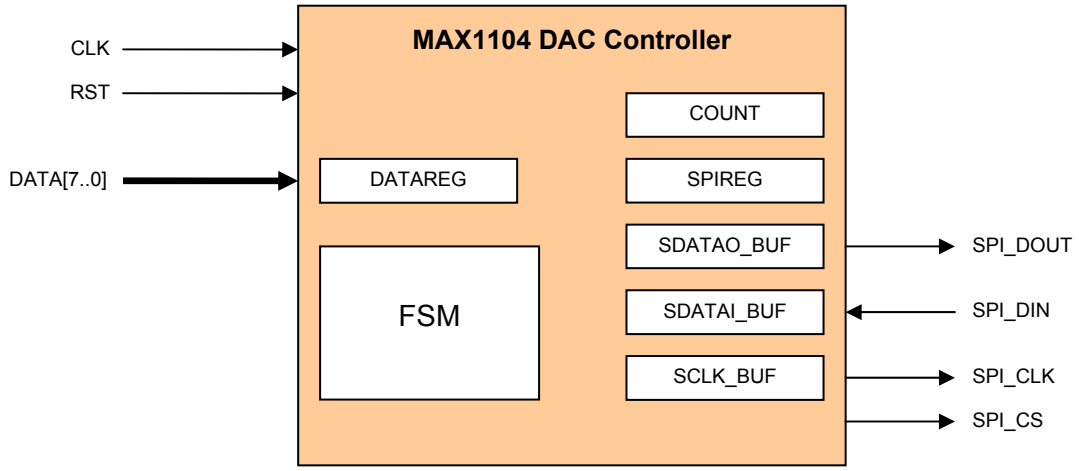

Figure 2. MAX1104_DAC block diagram.

Register Reset Values

Table 2 shows the values contained in the internal registers after an active external reset signal is received at the RST input of the device.

Table 2. Internal register reset values.

Register	Value after Reset
DATAREG	00h
COUNT	Unknown
SPIREG	Unknown
SDATAO_BUF	Unknown
SDATAI_BUF	Unknown
SCLK_BUF	Unknown

[1] As the MAX1104 CODEC to which this Controller is interfaced is rated at 6 MHz, SPI_SCLK should not exceed this frequency. As SPI_SCLK = 1/2CLK, the frequency for CLK should be limited to 12 MHz or less.

Placing a MAX1104_DAC Device in a Design

The Controller provides a simple interface to the on-board MAX1104 CODEC. Figure 3 shows an example of how the device is wired into a design.

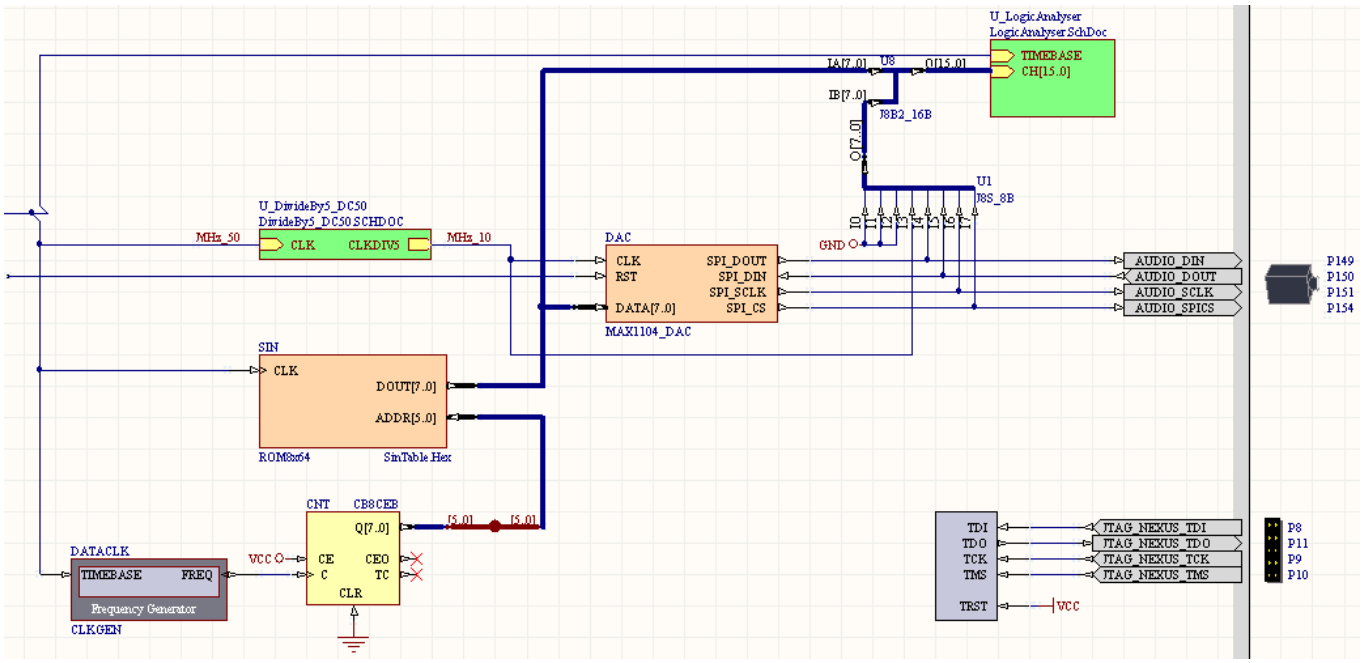

Figure 3. Providing the control interface to the on-board MAX1104 CODEC device.

In the example circuitry above, the MAX1104_DAC Controller takes, as input, sine wave data stored in a 64X8 block of ROM. Data is latched into the Controller (into the DATAREG register) on every falling edge of the CLK signal. This data is then sent to the MAX1104 CODEC device on the NanoBoard via the SPI Bus Interface.

Note that the frequency of the CLK signal is 10 MHZ. The SPI_CLK signal is half of this (5 MHz), which is below the maximum frequency rating of the MAX1104 CODEC (6 MH z).

Operation

At the heart of the Controller is an 8-state FSM (Finite State Machine), which is used to control the SPI Bus Interface – the communications medium between the Controller and the CODEC. The following outlines the sequence of data transfer during normal operation:

- Data is latched into the Controller's DATAREG register, from the DATA line, on every falling edge of the CLK signal. After a byte of data is latched, the Controller takes the SPI_CS signal Low, thus enabling the CODEC for data transfer.
- A configuration byte of data is then loaded into the SPIREG and sent out to the CODEC on the SPI_DOUT bus.
- The byte of data from the DATAREG register is then processed and sent to the CODEC, which latches the data in on the rising edge of the SPI_CLK.

Note: If communications between the Controller and the CODEC fail, issuing a reset (RST High) will send out a configuration byte to the CODEC, to re-establish the link.

Revision History

Date	Version No.	Revision
04-Feb-2004	1.0	New product release
26-May-2005	1.1	Updated for Altium Designer SP4
12-Dec-2005	1.2	Path references updated for Altium Designer 6
17-Mar-2008	2.0	Updated for Altium Designer Summer 08
30-Aug-2011	-	Updated template.