FPGA_STARTUPx Powerup Delay Unit

Summary

This document provides detailed reference information with respect to the powerup delay unit peripheral device.

The FPGA_STARTUPx Powerup Delay Unit is used to provide a delay of specified length, after the physical FPGA device has completed its powerup initialization sequence. This would enable, for example, a microcontroller within a design to be held within the reset state for a specific number of system clock cycles (after FPGA initialization) before entering the normal 'running' state. The design running within the FPGA device would therefore be started explicitly in the reset state.

Available Devices

The following three versions of the unit are available:

- **FPGA_STARTUP8** – Delay unit with a specified 8-bit delay
- **FPGA_STARTUP16** – Delay unit with a specified 16-bit delay
- **FPGA_STARTUP32** – Delay unit with a specified 32-bit delay

All devices in the FPGA_STARTUPx family can be found in the FPGA Generic integrated library (`FPGA Generic.IntLib`), located in the `\Library\Fpga` folder of the installation.

Functional Description

Symbol

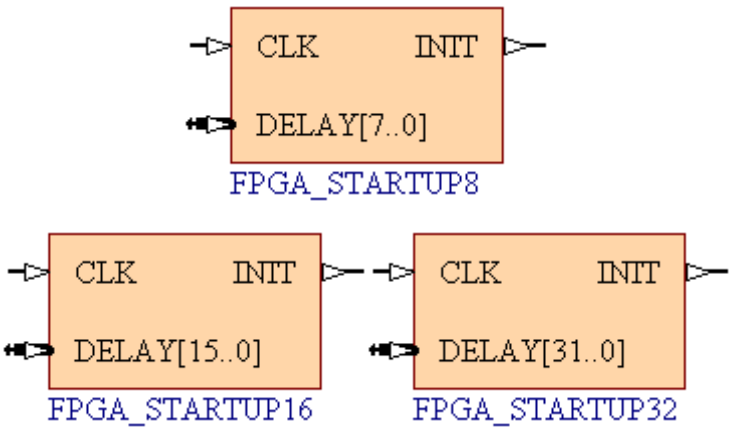

Figure 1. FPGA_STARTUPx Symbols

Pin Description

Table 1. FPGA_STARTUPx Pin description

Name	Type	Polarity/ Bus size	Description
CLK	I	Rise	External clock signal
DELAY	I	8[1] 16[1] 32[1]	The value assigned to this input determines the length of the delay generated, in terms of the number of cycles of the external clock signal wired to CLK.
INIT	O	Level	This signal remains High until the end of the specified delay, after which it goes Low and stays Low until the FPGA device is reinitialized.

Placing an FPGA_STARTUPx Device in a Design

The FPGA_STARTUPx family of devices provide a simple method of delaying the operation of a block of logic within a design. This is achieved by holding the design (or part thereof) in the reset state for a specified length of time, after the physical FPGA device has completed its initialization sequence. Figure 2 shows an example of how a Powerup Delay Unit is wired into a design.

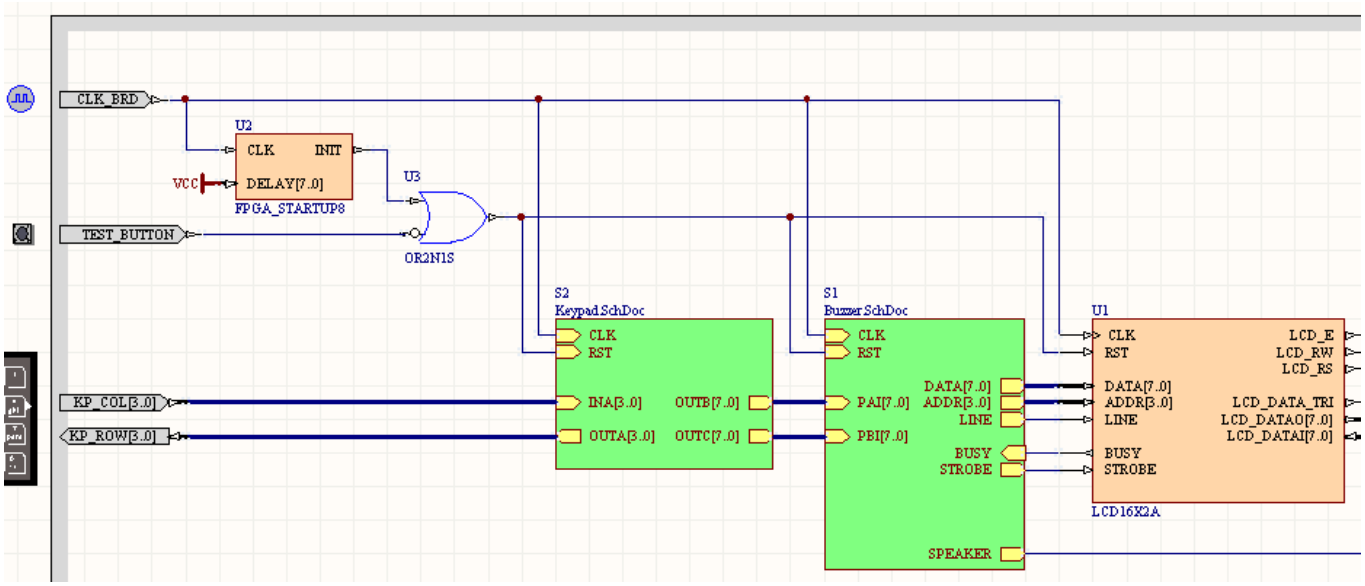

Figure 2. Using an FPGA_STARTUPx device to hold a design in the reset state for a specified time.

In the example circuit above, the Powerup Delay Unit used is the FPGA_STARTUP8. The output of the device has been ORed with the signal from the Test/Reset button on the NanoBoard and wired into the RST inputs of the various blocks within the design. In this example, the two sub-sheets involve TSK165B_D and TSK51A_D microcontrollers respectively.

After the physical FPGA device has been programmed with the design it will commence its initialization sequence. Once this has completed, both microcontrollers and the LCD Controller are held in the reset state for a duration specified by the DELAY input of the Powerup Delay Unit.

[1] 8 = FPGA_STARTUP8; 16 = FPGA_STARTUP16; 32 = FPGA_STARTUP32.

The DELAY bus in this case has been wired to a VCC bus power port. All eight bits are therefore set and the specified delay is 256. The design is therefore held in reset state for 256 cycles of the CLK signal, which in the example of Figure 2 is the NanoBoard clock.

After the 256 cycles have completed, the INIT output will go Low. Providing the Test/Reset button on the NanoBoard is not held down, the design will enter normal running operational mode.

Using Bus Constants to Determine the Delay

Any value for delay can be entered, up to the maximum supported for each device. Specification of a length for the delay that is not the maximum can be most easily achieved through the use of Bus Constants.

The constant value is specified in the net label for the bus and can be either decimal, binary or hexadecimal. Considering an FPGA_STARTUP16 device and a required delay of 342, the following entries for the bus net label could be used to define the constant:

- **Decimal**: `DELAY[15..0] <= 342`
- **Binary**: `DELAY[15..0] <= b101010110`
- **Hexadecimal**: `DELAY[15..0] <= $156`

Figure 3 illustrates the use of a bus constant to define the value for the DELAY input to an FPGA_STARTUP16 device.

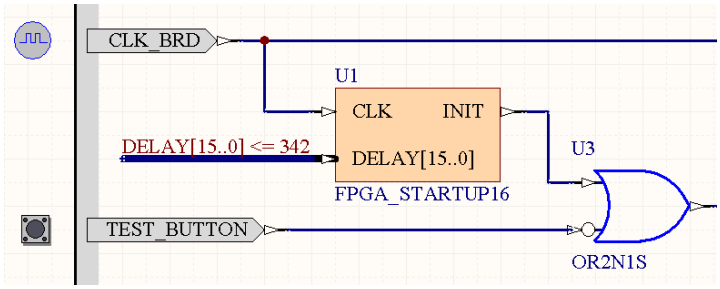

Figure 3. Specifying the value for DELAY using a bus constant.

Revision History

Date	Version No.	Revision
30-Jan-2004	1.0	New product release
26-May-2005	1.1	Updated for Altium Designer SP4
12-Dec-2005	1.2	Path references updated for Altium Designer 6
17-Mar-2008	2.0	Updated for Altium Designer Summer 08
30-Aug-2011	-	Updated template.